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by

G.H. BOOTH

ELECTRONICS LABORATORY

OTTAWA CANADA

DRTE REPORT NO. 1016 JUNE, 1959

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by

G.H. Booth

ABSTRACT -- The design and performance of a high frequency transistor amplifier with AGC, for operation over a wide temperature range is described. Although the procedure is related in particular to a 3 Mc/s IF amplifier for use in a Doppler Radar, the general principles are considered. These should be of interest to engineers concerned with other high frequency amplifier design requirements. The detection problems involved in dealing with a suppressed carrier signal of random phase are also considered.

1. INTRODUCTION

The development of transistorized Doppler navigation equipment necessitated the design of two 3 Mc/s intermediate-frequency transistor amplifiers with an overall gain of 60 db and a bandwidth of 100 kc/s. Operation over a temperature range of -55°C to +70°C, together with a constant output level at 200 mV rms ±5% over a 40 db variation in input signal was required. A noise figure of about 1 db was required for the complete IF amplifier. Since when the development was undertaken, use of available transistors had resulted in HF amplifiers with overall noise figures of 4 to 9 db, a low noise vacuum tube pre-amplifier was included. The gain of the complete amplifier then had to be the sum of the tube amplifier gain and the specified 60 db gain.

2. DESIGN APPROACH

2.1 CHOICE OF TRANSISTOR

By using a type of transistor for which the alpha cut-off frequency is about ten times the required operating frequency of 3 Mc/s, it was hoped that the complexities of neutralization and temperature stability would be minimized since both internal feedback and susceptive loading of the coupling circuits would be small. At the time of design the Philco Corporation surface barrier transistor, type SB100, was the only such transistor available.

2.2 NUMBER OF STAGES

Calculations showed that the average maximum available unilateralized gain per stage would be approximately 30 db (see Appendix I(iii). Temperature and automatic gain control requirements were such that a stabilizing loss, of some 10 db per stage as discussed in 2.6 below was necessary to provide sufficient centre frequency and bandwidth stability. Thus, when the coil insertion loss was taken into account, it was concluded that four transistor stages would be required.

2.3 CIRCUIT CONFIGURATION

The common emitter circuit was selected, since this configuration in a bandpass amplifier can result in higher gain than that obtainable in the common base connection. It has also been suggested that the common emitter circuit is likely to be the more stable of the two configurations[1].

2.4 TYPE OF INTERSTAGE COUPLING

Since no shape factor (skirt selectivity) was specified, single-tuned, unity-coupled interstage transformer coupling could be employed. This would expedite the desired method of neutralization (see 2.5) since simple, close-coupled, untapped transformer windings would fulfil all requirements.

2.5 NEUTRALIZATION

Neutralization, or more specifically unilateralization, is obtained by connecting a simple series RC network between collector and base. The network values are derived from the transistor parameters, by applying 4-terminal network theory (see Appendix I). In order that positive circuit elements may be used in the network, phase inversion is obtained by connecting the collector to the secondary of the unity coupled interstage transformer. The RC values are adjusted to accommodate the transformer turns ratio required for the desired degree of coupling mismatch.

2.6 TEMPERATURE COMPENSATION

Variations in transistor input and output parameters with varying temperature will result in changes in bandwidth and centre-frequency. To maintain these changes within reasonable limits some form of stabilization or compensation must be incorporated in the circuit design.

2.6.1 Bandwidth Stability

Acceptable bandwidth stability may be achieved by a number of means or combinations thereof.

(a) Parallel Stabilization

A stabilizing resistor is connected across the interstage coupling transformer. The value of this resistor is such that its loading effect is high compared with that due to the parallel combination of the input and output resistive components of the transistors to be coupled. Thus, changes both in the input and output resistive components may be swamped to any desired degree merely by decreasing the value of the stabilizing resistor at the expense of increased power loss.

(b) Series Stabilization

An effect similar to that in (a) above, may be achieved by suitably connecting a series stabilizing resistor. Here any desired degree of stability is obtained by increasing the value of the stabilizing resistor, again at the expense of increased power loss.

(c) Transformer Mismatch

Should either of the transistor input or output resistive components be more stable than the other, bandwidth stability can be made to depend mainly upon the more stable of the two by providing suitable transformer mismatch.

Experience has shown that in this particular design a combination of series stabilization and transformer mismatch provides the most economic means, in terms of total power loss, for stabilizing the amplifier bandwidth and centre-frequency.

The calculation of the relative values of the series stabilizing loss and mismatch loss for optimum bandwidth stability is shown in the Appendix II. It can be seen that in this design an approximately equal distribution of power loss between the series stabilizing resistor and mismatch loss provides optimum bandwidth stability at a given total power loss. Simultaneous changes of 50% in R_{22} and 10% in R_{11}, result in only 7% change in the total transformer loading.

2.6.2 Centre-Frequency Stability

The effect on the centre-frequency of changes in transistor input capacitance with temperature is also considerably reduced by the series stabilizing resistor. In this design, the transistor input capacitance contributes only about one-seventh of its original value to the required tuning capacity. The effect of change in output capacitance is unaltered. However, the output capacitance is small in comparison with the total tuning capacitance and hence, to some extent, the effect of changes in it is swamped.

The effect of changing transistor input and output capacitance is further reduced by the use of a suitable parallel combination of temperature-compensating tuning capacitors. Measurement has shown that the amplifier that uses uncompensated tuning capacitors has a positive temperature coefficient of 78 parts per million per ^{o}C. Capacitors that have nominal temperature coefficients of -750, -220, and +125 are available and a suitable combination to give the desired overall zero temperature coefficient can be arrived at by means of the following equations:

(i) $$NC_N - PC_p = KC$$

(ii) $$C = C_P + C_N$$

where K is the desired negative temperature coefficient of the combination,
C is the desired total tuning capacitance,
C_N is the required negative temperature coefficient capacitance,
C_P is the required positive temperature coefficient capacitance,
N is the available negative temperature coefficient,
P is the available positive temperature coefficient.

2.7 COIL INDUCTANCE

Having established the transformer turns ratio in terms of the required mismatch loss for optimum stability, the inductance of either the primary or secondary of the transformer remains to be calculated.

If identical circuit Q's are assumed at each interstage the required stage bandwidth is given by

$$BW = \frac{\text{Required Overall BW}}{\sqrt{2^{\frac{1}{n}} - 1}} \qquad \text{(Ref. 2)}$$

where n is the number of cascaded synchronously-tuned stages.

Thus the desired circuit Q is defined as

$$Q = \frac{f_o}{BW}$$

where f_o is the desired centre-frequency. The primary inductance of the interstage transformer is then calculated from the expression

$$L = \frac{R_T}{\omega}\left(\frac{1}{Q} - \frac{1}{Q_c}\right)$$

where R_T is the total external transformer loading referred to the primary,

Q_c is the relevant Coil Q,

$\omega = 2\pi f_o$. The expression is derived in Appendix III.

2.8 AGC CIRCUITRY

Automatic gain control is obtained by means of the circuit shown in Fig. 1.

With increasing output signal, V_{agc} (which is derived in the subsequent audio circuitry) is driven more negative, and this causes increased dc in the forward direction through the p-n junction diode. This results in increased diode ac conductance and hence, whilst reducing the fraction of the input signal delivered to the transistor, increases the loading on the tuned circuit. At the same time the emitter current is proportionally reduced by means of R_2 which results in decreased transistor input admittance, and hence reduced loading on the tuned circuit. Suitable adjustment of the ratio, R_2/R_3, therefore, can provide some compensation for the changed loading on the tuned circuit. The value of R_2/R_3 is derived in Appendix IV.

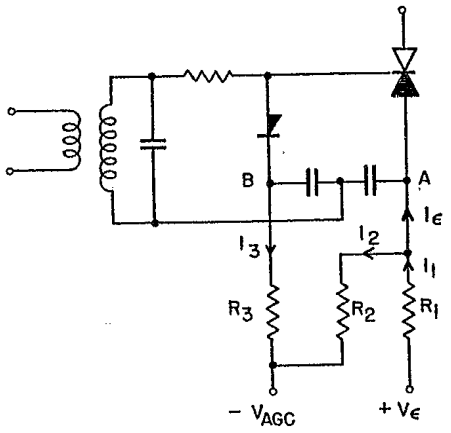

Fig. 1

The effect of changes in input susceptance is reduced to negligible proportions by the series stabilizing resistor and the swamping effect of the tuning capacitor. Changes in output susceptance also have negligible effect due to the favourable turns ratio and swamping effect of the tuning capacitor.

AGC is not applied to the last transistor stage because of three design considerations:

(1) The poorer swamping effect of the final tuning capacitor. (The lower tuning capacity in the detector stage results from the bandwidth and mismatch factors in the final coupling transformer design).

(2) Constant mixing performance will result only if no AGC is applied to this stage. (Re-injection of the 3 Mc/s carrier is performed at the base of the final transistor (see 2.9).

(3) The application of AGC to the final stage would have a deleterious effect upon the dynamic range of the receiver.

The AGC voltage requirements and output characteristic of this design are shown in Fig. 2.

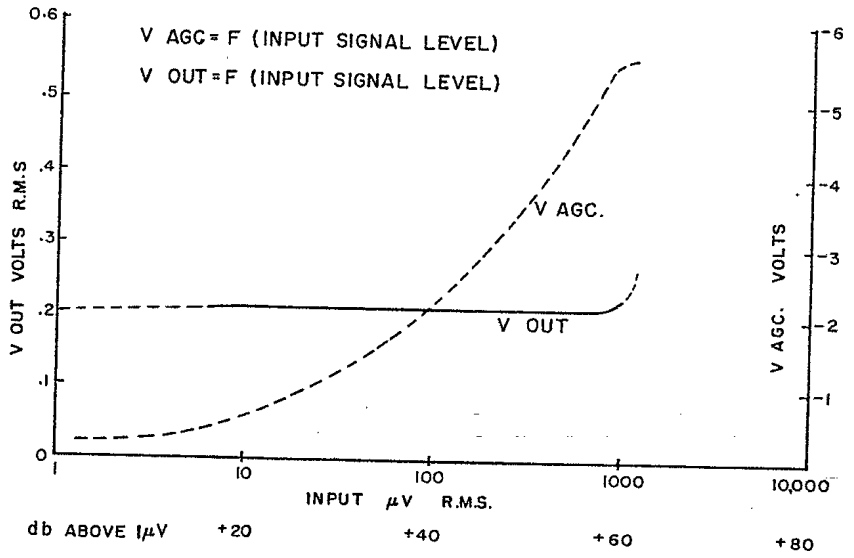

Fig. 2

2.9 MIXING

For design purposes, the Doppler signal presented to the IF amplifier may be considered as a double sideband, suppressed carrier signal. Re-injection of the 3 Mc/s carrier derived from the modulator unit[3] takes place at the base of the last transistor stage. For satisfactory harmonic suppression it has been shown in Appendix V, that the re-injected carrier signal E_c must be several times greater than E_s, the suppressed carrier signal level at the point of mixing. Furthermore, since the injected carrier for both the 'forward and backward looking' channels is derived from the same source, it is necessary that the signal due to one channel be considerably attenuated at the point of mixing in the other. For the selected value of $E_c = 5E_s$, which gives approximately 22 db of harmonic suppression in terms of the relative peak values (See Fig. 3), channel to channel attenuation of some 25 db is obtainable.

2.10 DEMODULATION

Demodulation is effected by a crystal diode in conjunction with a simple parallel RC circuit as detector load impedance. (For design details see Appendix VI).

3. CONCLUSIONS

The complete circuit diagram (Fig. 4) and parts list are appended.

(1) The required 200 mv. rms of audio output is obtainable from both amplifiers for input signals to the tube pre-amplifier of about 2 μv which represents a signal voltage of some 200 μ v at the input of the transistor amplifiers.

(2) The output signal level is maintained to within ±5% for a 40 db variation in the input signal, the variation in centre-frequency (mid-frequency, 3 db bandwidth) being not greater than

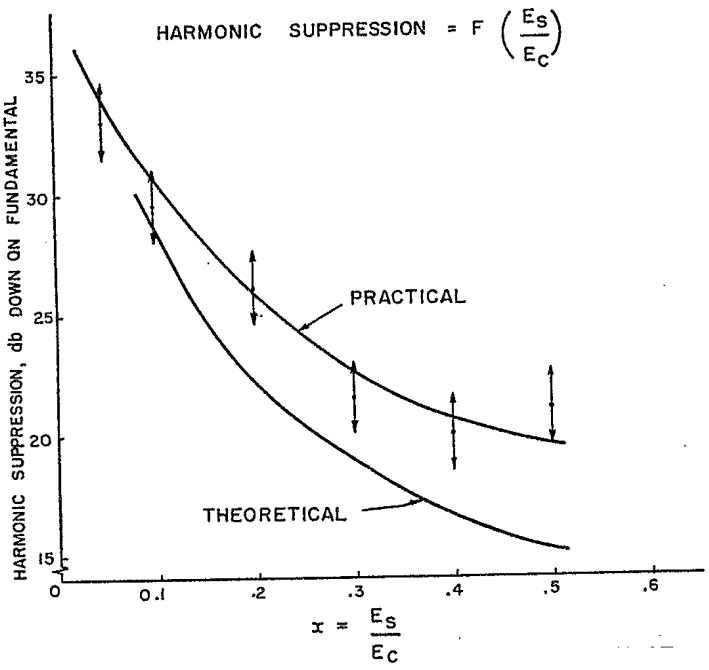

Fig. 3

±7.5 kc/s, or one quarter of one per cent of the carrier frequency. Bandwidth variation over the same range shows changes about the desired overall BW of 100 kc/s, of -38 kc/s to +30 kc/s and -60 kc/s to +34 kc/s respectively, for the two amplifiers, where the bandwidth increases with increasing gain control. A redetermination of the compensating ratio R_2/R_3 has resulted in improved bandwidth characteristics in a subsequent drift transistor amplifier where the ratio R_2/R_3 was individually determined by the measurement of β for the particular transistors involved.

(3) Satisfactory performance of a model has been obtained over the desired temperature range of $-55^{\circ}C$ to $+70^{\circ}C$.

(4) Two surface barrier type amplifiers have, to date (June, 1958), completed some 25 hours successful flying time at altitudes up to 20,000 feet. Overall system analysis appears to indicate, however, that some increase in specified sensitivity may be required at higher altitudes, and also that a more efficient mixing process may be desirable. The former requirement is being met by the use of the more recently available R.C.A. drift transistor. This will not only result in an electrically more rugged amplifier but may also offer the possibility of a transistorized, low noise, pre-amplifier. Finally, the possibility of a more efficient mixing process may be realized in a subsequent design by the use of a ring modulator in place of the simple carrier re-injection and diode demodulator of the present surface barrier type amplifier.

APPENDIX I

(i) Derivation of Feedback Circuit Admittance

Fig. 5 shows any linear active four-terminal network together with a transformer coupled output circuit.

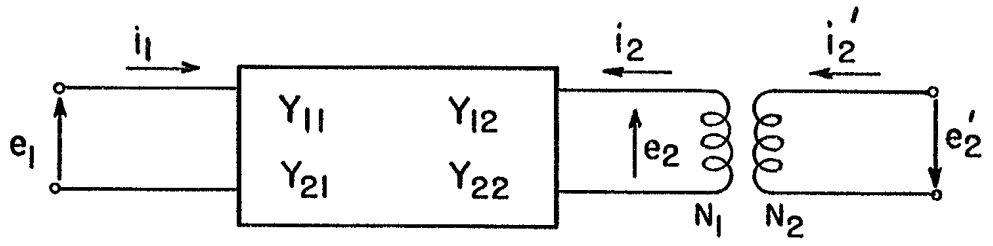

Fig. 5

The two circuit equations which completely describe the small signal operation of the transducer may be written in nodal form as follows: -

$$Y_{11}\, e_1 + Y_{12}\, e_2 = i_1 \qquad \ldots\ldots\ldots\ldots\ldots (1)$$

$$Y_{21}\, e_1 + Y_{22}\, e_2 = i_2 \qquad \ldots\ldots\ldots\ldots\ldots (2)$$

where Y_{11}, Y_{12}, Y_{21} and Y_{22} are the short circuit admittance parameters which are defined for the particular transducer involved by the two circuit equations (1) and (2). Also

$$e_2 = -e_2' \frac{N_1}{N_2} \qquad \ldots\ldots\ldots\ldots\ldots (3)$$

and

$$i_2 = i_2' \frac{N_2}{N_1} \qquad \ldots\ldots\ldots\ldots\ldots (4)$$

Substitute for e_2 and i_2 in equations (1) and (2) and obtain

$$Y_{11}\, e_1 - Y_{12}\, e_2' \frac{N_1}{N_2} = i_1 \qquad \ldots\ldots\ldots\ldots\ldots (5)$$

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and $$Y_{21}\, e_1 \frac{N_1}{N_2} - Y_{22}\, e_2' \left(\frac{N_1}{N_2}\right)^2 = i_2' \qquad \ldots\ldots\ldots\ldots\ldots (6)$$

Equations (5) and (6) describe the operation of the four-terminal network shown in Fig. 6, where

$$Y_{11}' = Y_{11} \qquad -Y_{22}' = Y_{22}\left(\frac{N_1}{N_2}\right)^2$$

$$Y_{12}' = -\frac{N_1}{N_2} Y_{12} \qquad Y_{21}' = Y_{21}\frac{N_1}{N_2}$$

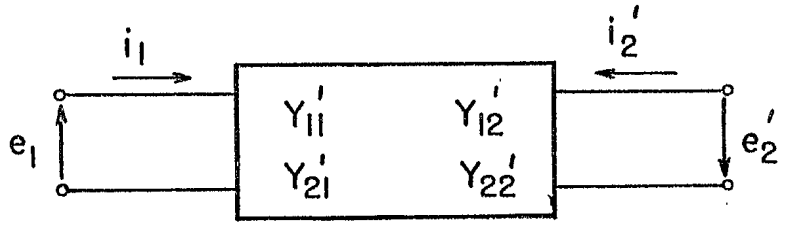

Fig. 6

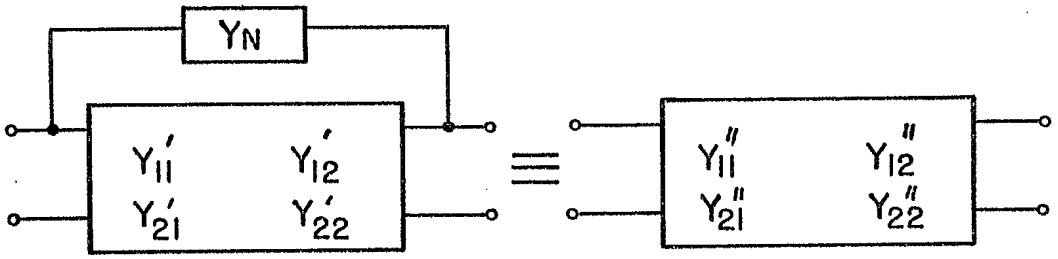

Fig. 7

Now connect a feedback element Y_N as shown in Fig. 7.

Then $$Y_{11}'' = Y_{11}' + Y_N \qquad Y_{21}'' = Y_{21}' - Y_N$$

$$Y_{12}'' = Y_{12}' - Y_N \qquad Y_{22}'' = Y_{22}' + Y_N$$

Hence $$Y_{11}'' = Y_{11} + Y_N \qquad Y_{21}'' = Y_{21}\frac{N_1}{N_2} - Y_N$$

$$Y_{12}'' = -\frac{N_1}{N_2} Y_{12} - Y_N \qquad Y_{22}'' = -Y_{22}\left(\frac{N_1}{N_2}\right)^2 + Y_N$$

For unilateralization,

$$Y_{12}'' = 0 \quad \text{i.e.} \quad Y_N = -\frac{N_1}{N_2} Y_{12} \qquad \ldots\ldots\ldots\ldots\ldots (7)$$

Equivalent circuit studies have shown that the reverse transfer admittance Y_{12} for a diffusion transistor is best represented by the circuit of Fig. 8. This circuit is equivalent to the configuration as shown in Fig. 9, where

$$R_1 = \frac{R_B^2}{R_A + R_B}, \qquad R_2 = \frac{R_A R_B}{R_A + R_B}$$

$$C_1 = C_A \left(\frac{R_A + R_B}{R_B} \right)^2$$

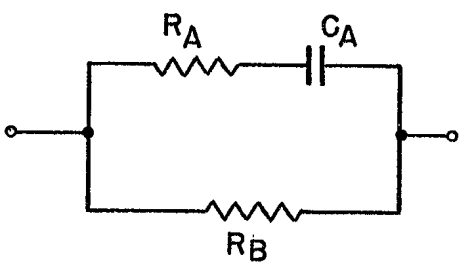

Fig. 8

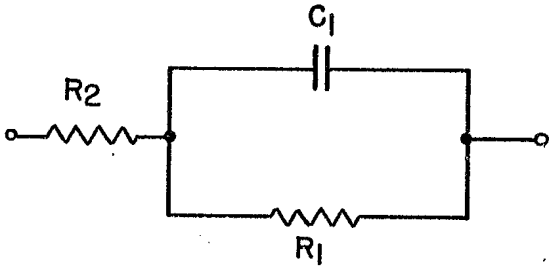

Fig. 9

Equivalent circuit values are such that at 3 Mc/s R_1 is very much larger than the reactance of C_1 and may therefore be neglected. Thus Y_N will consist of a simple series RC circuit (Fig. 10). At a given frequency this circuit is equivalent to the parallel combination R_2' C_1' where

$$Y_N = \frac{1}{R_2'} + j\omega C_1'$$

$$= -\frac{N_1}{N_2} Y_{12} \qquad \text{from equation (7)}$$

$$= -\frac{N_1}{N_2} G_{12} - \frac{N_1}{N_2} j\omega C_{12}$$

The unneutralized common emitter equivalent circuit admittance parameters G_{12}, C_{12} are calculated for an average transistor in terms of the measured small signal parameters from which the values of the common emitter equivalent circuit, Fig. 11, are derived as shown below.

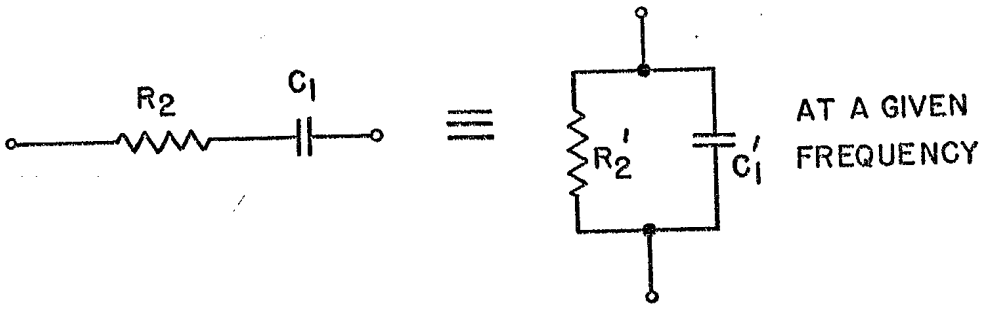

Fig. 10

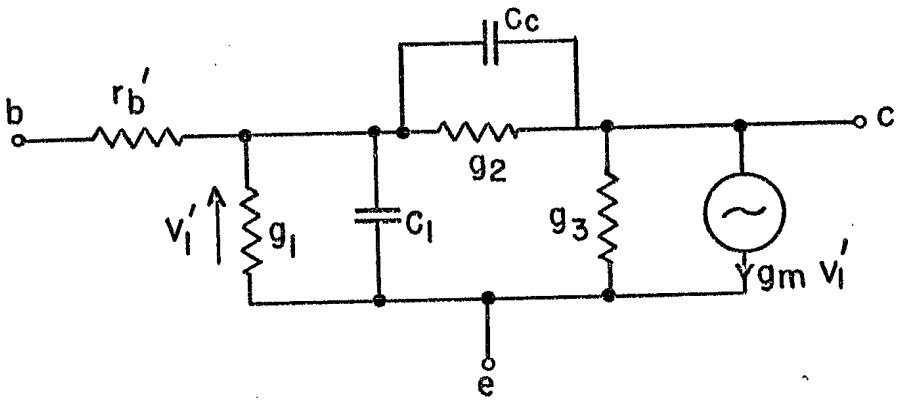

Fig. 11

Thus R_2', C_1' are obtained, and substitution in equation (8) gives the required series feedback circuit elements R_2, C_1.

$$R_2 = \frac{R_2'}{1 + \omega^2 C_1'^2 R_2'^2} \quad \text{and} \quad C_1 = \frac{1 + \omega^2 C_1'^2 R_2'^2}{\omega^2 C_1' R_1'^2} \qquad \ldots\ldots\ldots(8)$$

(ii) The Equivalent Circuit, Common Emitter Configuration

Fig. 11 shows the common emitter 'hybrid π' equivalent circuit in which each element is readily calculable from a knowledge of the small signal parameters measured at the required emitter current and collector voltage.

Using the usual nomenclature of the 'T' equivalent circuit, the required small signal parameters are r_e, r_b, r_c, α, C_c, r_b' and $f\beta_{co}$. The unknown elements of the 'hybrid π' equivalent circuit are then calculated as follows(1):

$$g_1 = \frac{1 - \alpha_o}{r_d} \qquad \text{where } r_d = r_e + r_b'' (1 - \alpha_o)$$

$$(r_b'' = r_b - r_b')$$

$$g_2 = \frac{r_e}{r_c r_d}$$

$$g_3 = \frac{r_b''}{r_c r_d}$$

$$g_m = \frac{\alpha_o}{r_d}$$

At $f\beta_{co}$ $\qquad \frac{2\pi f \beta_{co} \cdot C_1}{g_1} = 1 \qquad$ i.e. $C_1 = \frac{g_1}{\omega \beta_{co}}$

The short-circuit admittance parameters can now be calculated in terms of the equivalent circuit values, the admittance parameters being given by the following expressions[4]:

$$G_{11} = \frac{g_b g_1}{g_b + g_1} \left(\frac{1 + \omega^2 \tau_1 \tau_2}{1 + \omega^2 \tau_2^2} \right)$$

$$G_{21} = \frac{g_b}{g_1 + g_b} \left(\frac{g_m - \omega^2 \tau_2 C_c}{1 + \omega^2 \tau_2^2} \right)$$

$$G_{22} = g_2 + g_3 + \frac{g_m}{g_1 + g_b} \left(\frac{g_2 + \omega^2 \tau_2 C_c}{1 + \omega^2 \tau_2^2} \right)$$

$$G_{12} = -\frac{g_b}{g_1 + g_b} \left(\frac{g_2 + \omega^2 \tau_2 C_c}{1 + \omega^2 \tau_2^2} \right)$$

$$C_{11} = \left(\frac{g_b}{g_1 + g_b} \right)^2 \left(\frac{C_1}{1 + \omega^2 \tau_2^2} \right)$$

$$C_{21} = - \frac{g_m g_b}{(g_1 + g_b)^2} \left(\frac{C_1}{1 + \omega^2 \tau_2^2} \right)$$

For maximum power transfer to the load

$$g_L = g_{out} \quad \text{where } g_L \text{ is the load conductance.}$$

$$\text{Then maximum available power out} = \frac{V_1^2 \, g_m'^2}{4 g_{out}}$$

$$\text{and input power} = V_1^2 \, g_{in} \, .$$

Thus the maximum available unilateralized gain per stage is given by

$$\frac{\text{maximum available power out}}{\text{input power}} = \frac{g_m'^2}{4 g_{in} g_{out}} \, .$$

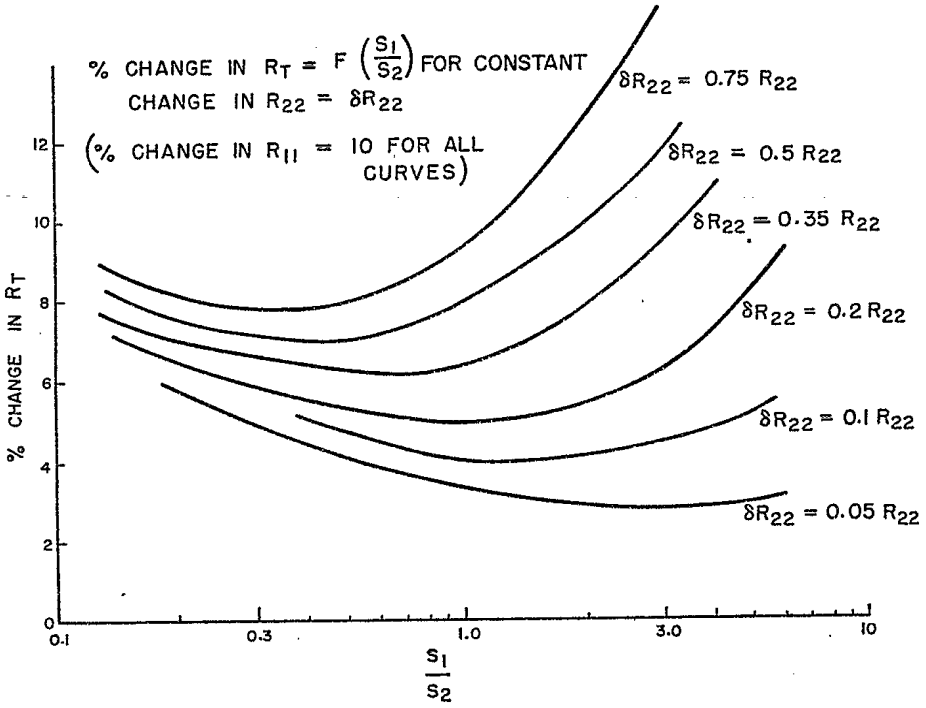
% CHANGE IN R_T = F $\left(\frac{S_1}{S_2}\right)$ FOR CONSTANT CHANGE IN R_{22} = δR_{22}
(% CHANGE IN R_{11} = 10 FOR ALL CURVES)
δR_{22} = 0.75 R_{22}
δR_{22} = 0.5 R_{22}
δR_{22} = 0.35 R_{22}
δR_{22} = 0.2 R_{22}
δR_{22} = 0.1 R_{22}
δR_{22} = 0.05 R_{22}
% CHANGE IN R_T
0
2
4
6
8
10
12
0.1
0.3
1.0
3.0
10
$\frac{S_1}{S_2}$

Fig. 13

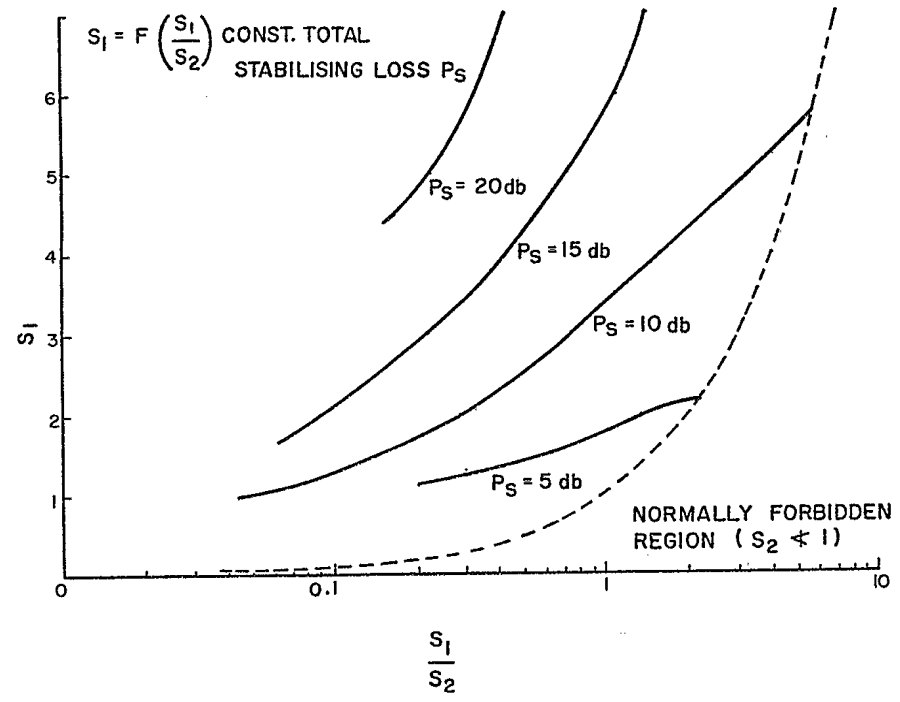
S_1 = F $\left(\frac{S_1}{S_2}\right)$ CONST. TOTAL STABILISING LOSS P_S
P_S = 20db
P_S = 15 db
P_S = 10 db
P_S = 5 db
NORMALLY FORBIDDEN REGION ($S_2 < 1$)
S_1
0
1
2
3
4
5
6
0.1
1
10
$\frac{S_1}{S_2}$

Fig. 14

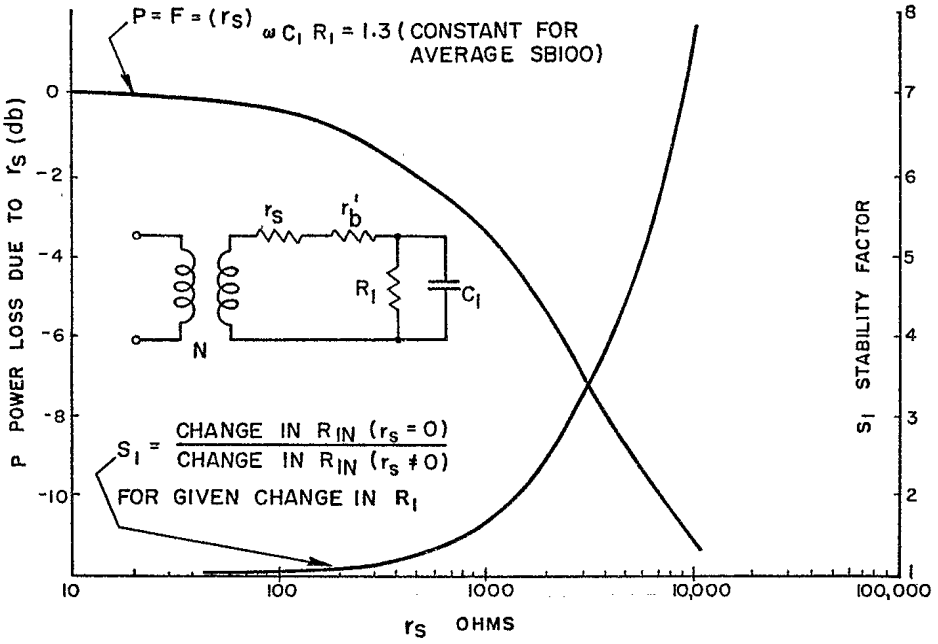
P = F = (rS) ω C1 R1 = 1.3 (CONSTANT FOR AVERAGE SB100)
P POWER LOSS DUE TO rS (db)
0
-2
-4
-6
-8
-10
rS
r'b
R1
C1
N
S1 = CHANGE IN RIN (rS = 0) / CHANGE IN RIN (rS ≠ 0)
FOR GIVEN CHANGE IN R1
S1 STABILITY FACTOR
8
7
6
5
4
3
2
1
10
100
1000
10,000
100,000
rS OHMS

Fig. 15

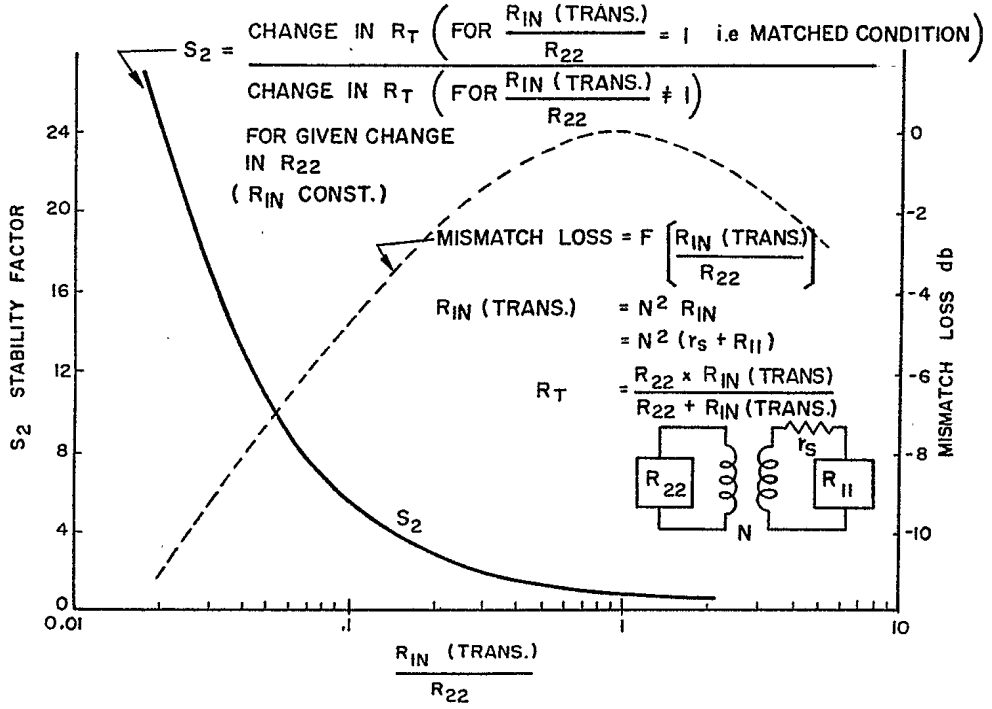
S2 = CHANGE IN RT (FOR RIN (TRANS.) / R22 = 1 i.e MATCHED CONDITION) / CHANGE IN RT (FOR RIN (TRANS.) / R22 ≠ 1)
FOR GIVEN CHANGE IN R22 (RIN CONST.)
MISMATCH LOSS = F [RIN (TRANS.) / R22]
RIN (TRANS.) = N2 RIN
= N2 (rS + RII)
RT = R22 × RIN (TRANS) / R22 + RIN (TRANS.)
S2 STABILITY FACTOR
24
20
16
12
8
4
0
S2
R22
rS
RII
N
MISMATCH LOSS db
0
-2
-4
-6
-8
-10
0.01
.1
1
10
RIN (TRANS.) / R22

Fig. 16

The value of S_1 is then read directly from the relevant curve of Fig.14 where S_1 is shown plotted as a function of S_1/S_2 for constant total stabilizing loss P_s. S_2 is found by simple calculation and the required values of r_s and the ratio $\frac{R_{in}\,(trans)}{R_{22}}$ (and hence the turns ratio N) are read directly from the Figs. 15 and 16 respectively.

Fig. 15 shows also the power loss in the series stabilizing resistor as a function of the value of the stabilizing resistor and Fig. 16 illustrates the power loss due to the mismatch.

Figs. 13 to 16 are all based on values for an average surface barrier transistor type SB100 selected from a sample of 25.

As an example, the calculation of r_s and N for this design will be shown.

Indications are such that the percentage change in R_{22} is approximately $\pm 50\%$, whereas the percentage change in R_{11} is only about $\pm 10\%$ over the required temperature range. Thus, with reference to Fig. 13,

$$\delta R_{22} = 0.5\ R_{22}$$

and for minimum change in R_T,

$$S_1/S_2 \simeq 0.425.$$

For a total stabilizing loss of 10 db, i.e., one-third of the maximum available unilateralized gain per stage, $S_1 = 2.37$ (from Fig. 14).

Fig. 15 then gives $r_s = 2K\Omega$.

Using $r_s = 1.8\ K\Omega$ (next lower $\pm 10\%$ R.M.A. standard value)

$$S_1 = 2.2,$$

and thus

$$S_2 = \frac{2.2}{0.425} = 5.175.$$

From Fig. 16

$$\frac{R_{in}\,(trans)}{R_{22}} = 0.109$$

$$R_{in}\,(trans) = 0.109 \times 13.5 \times 10^3$$

$$= 1.47 \times 10^3$$

$$= N^2 R_{in}$$

$$N^2 = \frac{1.47 \times 10^3}{r_s + R_{11}}$$

$$= \frac{1.47}{1.8 + 1.5}$$

$$= 0.445$$

and $N = 0.667$ or $1:1.5$.

And total loss = series stabilizing loss + mismatch loss

= 5 + 4.5 (from Figs. 15 and 16)

= 9.5 db,

the decrease of 0.5 db from the intended total stabilizing loss being due to the selection of a standard value for r_s lower than that indicated by the analysis.

APPENDIX III

DERIVATION OF AN EXPRESSION FOR COIL INDUCTANCE

It was shown previously that

$$R_T = \frac{R_{22} \times R_{in}\,(\text{trans})}{R_{22} + R_{in}\,(\text{trans})}$$

If the loading effect due to the equivalent parallel circuit resistance of the coil is included, then the total primary loading becomes

$$R_T' = \frac{R_T R_p}{R_T + R_p}$$

where R_p = equivalent parallel circuit resistance of the coil

$$= \omega L Q_c$$

the terms of which were defined previously.

Also $$BW = \frac{f_o}{Q}$$

and $$Q = \frac{R_T'}{\omega L}$$

Therefore, by substitution,

$$L = \frac{R_T' BW}{\omega f_o}$$

$$= \frac{R_T R_p BW}{(R_T + R_p)\,\omega f_o}$$

$$= \frac{R_T \omega L Q_c BW}{(R_T + \omega L Q_c)\,\omega f_o}$$

and hence $$\omega L Q_c = \frac{R_T Q_c BW}{f_o} - R_T$$

and

$$L = \frac{R_T}{\omega}\left(\frac{BW}{f_o} - \frac{1}{Q_c}\right)$$

$$= \frac{R_T}{\omega}\left(\frac{1}{Q} - \frac{1}{Q_c}\right)$$

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APPENDIX IV

AGC CIRCUITRY: CALCULATION OF RATIO R_2/R_3 FOR CONSTANT INPUT CONDUCTANCE

Fig. 17 shows the variation of input conductance, G_D and G_T, with change in diode and emitter current for a Transitron diode, type 1N273 and a Philco surface barrier transistor, type SB100, where $G_T = G_{11}$, and the equations of the two curves are approximately

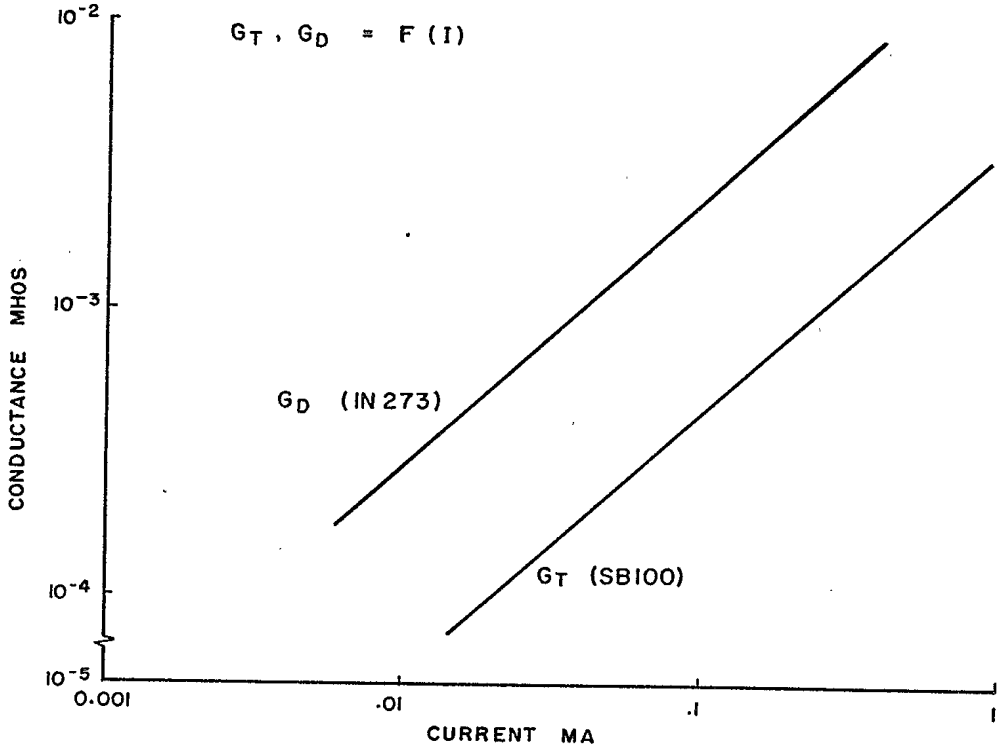

Fig. 17 - Diode and Transistor Input Conductance as a Function of Current

(1) $G_T = 3.75 \times 10^{-3} I_\epsilon + 1.55 \times 10^{-5}$

(2) $G_D = 2.19 \times 10^{-2} I_D + 1.1 \times 10^{-5}$.

I_ϵ, I_D are expressed in mA.

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For constant total input conductance it is required that

$$G_{tot} = G_T + G_D = \text{constant.}$$

Point A, Fig. 1 is held very near to ground potential by the clamping action of the emitter. Thus

$$I_1 = \frac{V_\epsilon}{R_1} = \text{constant}$$

and similarly $$I_2 = \frac{V_{agc}}{R_2} .$$

Point B also is held very near ground potential by the clamping action of the diode.

Thus $$I_3 = \frac{V_{agc}}{R_3}$$

Now $$I_\epsilon = I_1 - I_2$$

and $$I_D = I_3.$$

Hence, substituting in equations (1) and (2),

$$G_T = 3.75 \times 10^{-3} (I_1 - I_2) + 1.55 \times 10^{-5}$$

$$= 3.75 \times 10^{-3} \times I_1 + 1.55 \times 10^{-5} - 3.75 \times 10^{-3} \times \frac{V_{agc}}{R_2}$$

and $$G_D = 2.19 \times 10^{-2} \times \frac{V_{agc}}{R_3} + 1.1 \times 10^{-5}$$

which gives

$$G_{tot} = G_T + G_D$$

$$= 3.75 \times 10^{-3} \times I_1 + (1.55 \times 1.1)\ 10^{-5} +$$

$$\left(\frac{2.19 \times 10^{-2}}{R_3} - \frac{3.75 \times 10^{-3}}{R_2} \right) V_{agc}$$

$$= \text{constant for } \frac{R_2}{R_3} = \frac{3.75}{2.19} \times 10^{-1}$$

$$\simeq 0.17.$$

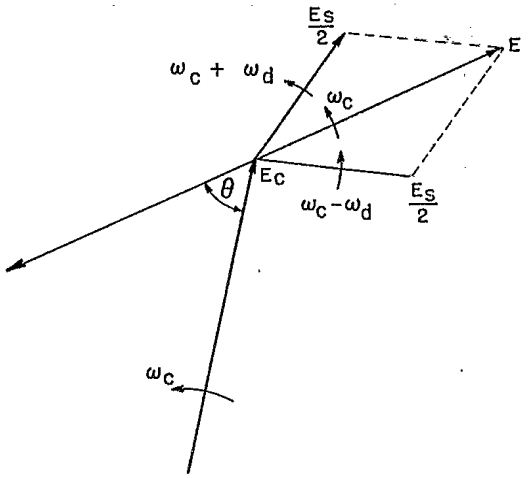

Fig. 18

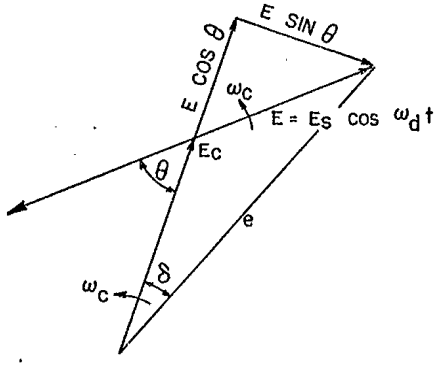

Fig. 19

Thus the resultant envelope is given by

$$e = \sqrt{X^2 + Y^2}$$

which represents a dc term and an infinite series of harmonic components.

The ratio of the fundamental content to the total subsequent harmonic content is required. This may be written as

$$\frac{A_{n=1}}{\sum_{n=1}^{n=\infty} A_n}$$

for various values of $x = E_s/E_c$ and then averaged for all Θ from 0 to $\pi/2$. A_n is the Fourier coefficient of the nth harmonic component of the resultant envelope

$$e = \sqrt{X^2 + Y^2}$$

$$= E_c \left(1 + \frac{x^2}{2} + \frac{x^2}{2} \cos 2\omega_d t + 2x \cos \omega_d t \cos \Theta\right)^{1/2}.$$

Evaluation of the Fourier coefficients averaged for all Θ from 0 to $\pi/2$ by the usual integral methods leads to some considerable difficulty because the expression involves a half power.

Alternatively, the binominal expansion for e will yield the required Fourier coefficients. However, the resultant series is divergent, the nth term contributes to all the Fourier coefficients up to and including A_{2n}, so that any reasonably calculable approximation is rendered invalid.

Therefore, consider the in-phase compnent alone. This would have a peak value E_{pk} after mixing and demodulation given by

$$E_{pk} = E_s \cos \Theta$$

which has an average value E_{pk} (aver.) for all Θ from 0 to $\pi/2$ where

$$E_{pk}(\text{aver.}) = \frac{2}{\pi} \int_0^{\frac{\pi}{2}} E_s \cos \Theta \, d\Theta$$

$$= \frac{2E_s}{\pi} \qquad \ldots\ldots\ldots\ldots\ldots (1)$$

The quadrature component alone, if combined with the carrier E_c, would have a resultant e_H where

$$e_H = (E_c^2 + E_s^2 \cos^2 \omega_d t \sin^2 \Theta)^{1/2}$$

$$= E_c (1 + x^2 \cos^2 \omega_d t \sin^2 \Theta)^{1/2}$$

which is shown plotted together with

$$X = E_c + E_s \cos \omega_d t \cos \Theta,$$

the in-phase component in Fig. 20.

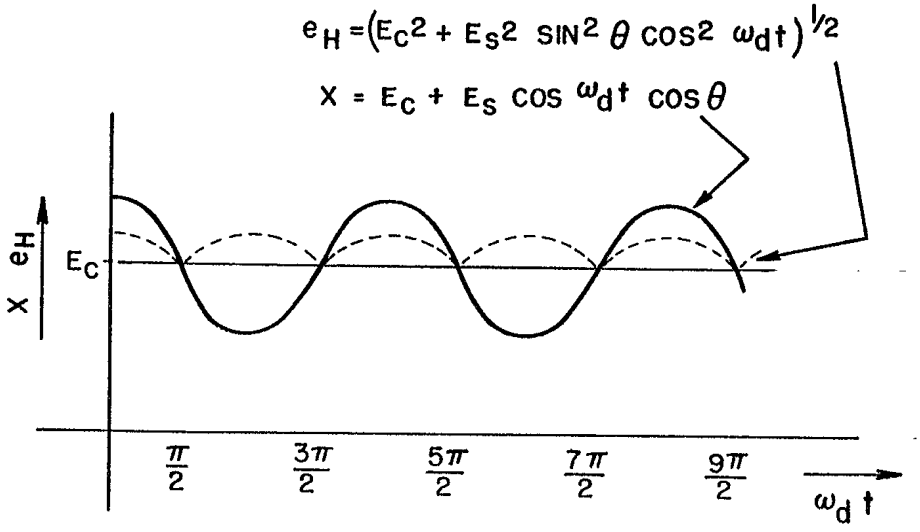

Fig. 20

After demodulation, the contribution due to the quadrature component alone would have a peak value E_{Hpk} where

$$E_{Hpk} = e_H - E_c$$

$$= E_c [(1 + x^2 \sin^2 \Theta)^{1/2} - 1] \quad \text{(see Fig. 21)}$$

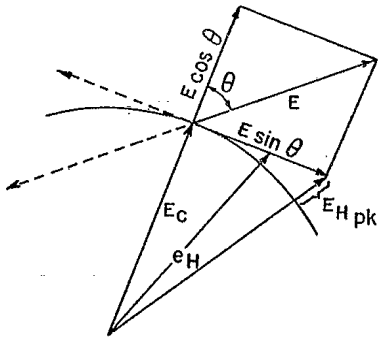

Fig. 21

This has an average value for all Θ from 0 to $\pi/2$ given by

$$E_H pk\,(aver.) = \frac{2E_c}{\pi} \int_0^{\frac{\pi}{2}} [(1 + x^2 \sin^2 \Theta)^{1/2} - 1)]\, d\Theta$$

$$= -\frac{2E_c}{\pi} \int_{\phi=\frac{\pi}{2}}^{\phi=0} [\sqrt{1 + x^2}(1 - \frac{x^2}{1 + x^2} \sin^2 \phi)^{1/2} + 1]\, d\phi$$

where $\sin \phi = \cos \Theta$

$$= \frac{2E_c}{\pi} \int_0^{\frac{\pi}{2}} [\sqrt{1 + x^2}\,(1 - \frac{x^2}{1 + x^2} \sin^2 \phi)^{1/2} - 1]\, d\phi$$

Now

$$E(k) = \int_0^{\frac{\pi}{2}} (1 - \frac{x^2}{1 - x^2} \sin^2 \phi)^{1/2}\, d\phi$$

is the Legendre form of the complete elliptic integral of the second kind for $k = \frac{x}{\sqrt{1 + x^2}}$ where $0 \leq k < 1$ and is obtainable from Legendre's Tables[6], for $\alpha = 0$ to $\pi/2$ where $\alpha = \sin^{-1} k$.

Thus E(k) can be tabulated as a function of x, from which is obtained,

$$E_{Hpk}\,(aver.) = \frac{2E_c}{\pi} [\sqrt{1 + x^2} \cdot E(k) - \frac{\pi}{2}]$$

This is to be compared for all values of x with

$$E_{pk}\,(aver.) = \frac{2E_s}{\pi} \qquad \text{(see Equation (1))}$$

Thus, in terms of the relative peak values of the fundamental and the total subsequent harmonic content, the harmonic suppression in db as a function of x is given by

$$F(x) = 20 \log_{10} \frac{E_{pk}}{E_{Hpk}}$$

$$= 20 \log \frac{x}{\sqrt{1 + x^2} \cdot E(k) - \frac{\pi}{2}} \qquad \text{which is shown in Fig. 3.}$$

APPENDIX VI

DEMODULATION: DETECTOR LOAD IMPEDANCE DESIGN

The detector load impedance consists of a simple parallel RC combination.

A suitable time constant for the RC circuit was determined by consideration of the following expressions:

1) If diagonal dipping is not to occur the following relation must hold

$$\frac{X_{cs}}{R} \geq \frac{m}{\sqrt{1 - m^2}} \qquad \text{(reference 7)}$$

where X_{cs} is the reactance of the shunt capacity in the detector time constant at the highest modulating frequency. R is the resistance in the detector time constant and m is the fractional modulation which is given by

$$m = \frac{E_{max} - E_o}{E_o}$$

where E_{max} and E_o are the maximum and average amplitudes of the modulation envelope.

Now

$$E_{max} = E_c + E_s = 5E_s + E_s = 6E_s \quad \text{(from 2.9)}$$

and

$$E_o = E_{max} - E_s$$

$$= 5E_s$$

and hence

$$m = 0.20.$$

This establishes a maximum value for m which is obtainable only for correct phase re-injection of the carrier. The correct phase of the re-injected carrier in a suppressed carrier system for optimum undistorted amplitude modulated output is that phase which the carrier would have obtained at the point of mixing had it not been suppressed. In the Doppler application it has been seen that (Appendix V) the phase of the signal at the point of mixing is entirely random. However, in this calculation the maximum permissible value of shunt capacitance is limited by the maximum value of m experienced at any given time; incorrect phase re-injection of the carrier results in lower fractional modulation and hence higher permissible shunt capacitance.

2) Also, for negligible carrier frequency ripple make

$$RC > 10T$$

where T = period of one cycle of the carrier.

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The maximum acceptable value of R is set at 10 kΩ due to the stabilizing requirements of the emitter follower in the subsequent circuitry, since the emitter follower is dc coupled to the detector load impedance.

Thus a range of values are available for C (from 330 to 3825 pf, the value 3825 pf being determined by assuming a maximum Doppler frequency of 20 kc/s). As the determining factor was the physical dimensions of the silver-mica capacitors available at the time of construction, a value of 500 pf was selected.

APPENDIX VII

PARTS LIST

TRANSISTORS

4 Philco SB 100 and clips
1 Texas 2N 302

TRANSFORMERS

T_1 Pri. Ind. 3.25 μH, Turns Ratio 1:1.5, close-coupled, tunable
T_2 Pri. Ind. 4.5 μH, Turns Ratio 1:2.5, close-coupled, tunable

DIODES

4 Transitron 1N273

RESISTORS

R_1	1.8 KΩ	1/10 watt
R_2	12 KΩ	"
R_3	68 KΩ	"
R_4	12 KΩ	"
R_5	3.9 KΩ	"
R_6	18 KΩ	"
R_7	10 KΩ	"
R_8	3.3 KΩ	"

CAPACITORS

C_1	.01 μF	Aerovox ceramic
C_2	3x.05 μF	Ceramic
C_3	275 pf	Corning glass P125
C_4	82 pf	Hi-Kap ceramic tubular N750
C_5	50 pf	Corning glass P125
C_6	20 pf	Hi-Kap ceramic tubular N750
C_7	2.2 pf	Hi-Kap ceramic tubular
C_8	1.1 pf	Hi-Kap ceramic tubular
C_9	500 pf	Silver-mica.

4. ACKNOWLEDGMENTS

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