Image Cover Sheet

CLASSIFICATION	SYSTEM NUMBER
UNCLASSIFIED	506667

TITLE

IMPLEMENTATION OF A DIGITAL PHASE-LOCKED LOOP ON A VECTOR PROCESSOR

System Number:

Patron Number:

Requester:

Notes:

DSIS Use only:

Deliver to:

IMPLEMENTATION OF A DIGITAL PHASE-LOCKED LOOP ON A VECTOR PROCESSOR

Brian H. Maranda

Defence Research Establishment Atlantic,
P.O. Box 1012, Dartmouth, NS, Canada B2Y 3Z7

Abstract - **A digital phase-locked loop (DPLL) has been implemented as part of a demodulator that reproduces data signals telemetered over a radio link. This paper describes the design of the DPLL and its implementation on a vector-processing card for real-time operation; also described is the automatic gain control (AGC) placed in front of the DPLL.**

I. INTRODUCTION

A device used in the armed forces of many countries today is the sonobuoy, an expendable sensor that is dropped from an aircraft to the ocean surface. Sound signals received by the sonobuoy's transducers are telemetered via an FM radio link to the aircraft, where the signals are monitored.

In one type of sonobuoy, called the DIFAR buoy, there are three acoustic channels to be transmitted over the radio link: one channel obtained from an omni-directional hydrophone and two channels from directional sensors (dipoles). These three channels are multiplexed into a composite signal for transmission over the radio link, and this composite signal must be demultiplexed at the receiver in order to retrieve the three constituent signals for subsequent analysis.

The spectrum of the composite signal is depicted in Fig. 1. The omni channel is placed at baseband and can be extracted by simple lowpass filtering. The two directional channels are double-sideband modulated by two 15-kHz carriers in quadrature and then summed; we shall refer to the resultant signal as the QDSB signal. One of the 15-kHz carriers is inserted into the composite signal to act as a pilot. Also inserted into the composite signal is a 7.5-kHz pilot, whose function will be described shortly.

For the purpose of demodulation, two 15-kHz reference carriers are generated locally at the receiver, one synchronous with the 15-kHz pilot and the other in quadrature. By mixing the composite signal with these reference carriers and lowpass filtering, the two directional channels are retrieved. However, it is hard to acquire and track the 15-kHz pilot owing to (i) an allowed offset of ± 50 Hz from the nominal frequency, and (ii) the close proximity of the signal sidebands.

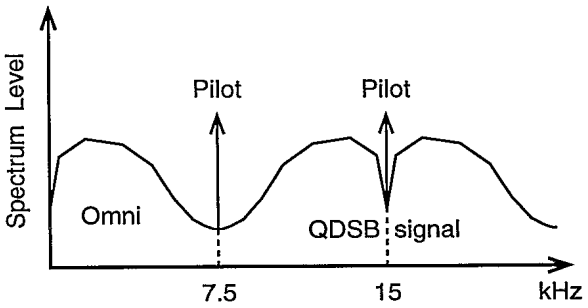

Figure 1. Spectrum of the composite signal.

The 7.5-kHz pilot facilitates demodulation, as it has been placed in a "quiet" part of the spectrum where it can be easily acquired and tracked. (The pilot in a commercial stereo FM signal is similarly located [1].) The 7.5-kHz pilot is produced from the 15-kHz pilot in the multiplexer by a frequency divider, and is at exactly half the true frequency of the 15-kHz pilot, i.e., is within ± 25 Hz of the nominal 7.5 kHz. The frequency of the pilot may vary at a rate of 1 Hz/sec within this range.

The rest of the paper focusses on the method for producing a local reference carrier synchronous with the 7.5-kHz pilot. Descriptions of the subsequent demodulation stages, such as doubling the frequency of the 7.5-kHz reference carrier to locate the pilot at 15 kHz, are omitted for brevity.

II. CHOICE OF ALGORITHM

The main task in generating the 7.5-kHz reference carrier is estimating the phase and frequency of a sinusoid in noise. The standard DSP estimators are based on the fast Fourier transform, or, more generally, on the discrete Fourier transform (DFT). For a fixed-frequency tone, there can be no doubt that DFT methods provide near-optimal estimates of phase and frequency [2]. Nevertheless, a decision was made to use a DPLL.

One of the determining factors was that the pilot frequency may vary as a function of time (up to 1 Hz/sec), and tracking a variable-frequency tone using the DFT is not a cut-and-dried procedure. Also, DFT methods are block-based, and it would be necessary to piece together a reference waveform that is phase-continuous across block bound-

aries, or produce an algorithm that did this implicitly. The DPLL has the advantage that it produces the desired reference waveform sample by sample, and the question of how to construct a phase-continuous reference never arises.

However, the target hardware for the demultiplexer implementation was a VME vector card based on Intel i860 chips. The DPLL is a recursive, or feedback, structure, meaning that the output from one time interval is used as the input for the next. Unfortunately, recursive algorithms are poorly matched to vector processors, which obtain their speed by pipelining the arithmetic operations: The pipeline cannot be filled, since the input is unknown until the output is valid. The method used to gain efficiency was to implement the DPLL at baseband and decrease the sampling rate; the DSP operations used in performing the basebanding are very efficient on a vector processor.

III. OVERVIEW OF LOCAL CARRIER GENERATION

Figure 2 shows a schematic of the sub-system used to generate the local 7.5-kHz reference carrier. The following subsections step through the schematic stage by stage, with most of the attention directed to the DPLL design. It is assumed that the composite signal has been digitized at a 48-kHz sampling rate by an analog-to-digital converter.

A. *FREQUENCY TRANSLATION*

The DPLL is implemented at baseband, and so must be surrounded by frequency translators. The front-end translator is a complex demodulator, consisting of a mixer followed by a lowpass filter. The mixer frequency is 7.5 kHz, yielding a baseband pilot in the range ±25 Hz. The function of the back-end 7.5-kHz remodulator is to translate the DPLL output back to the original frequency band. The carrier estimate is complex-valued, containing both an inphase carrier reference and its quadrature.

The lowpass filter is several kHz wide (one-sided), and is sufficiently narrow to allow decimation by a factor of 10. This filter is an FIR filter with 59 coefficients, and is also used as the anti-imaging filter at the back-end 1:10 interpolator. Although Fig. 2 shows the down- and up-sampling as being performed separately from the filters, this division is purely conceptual. For example, polyphase filters were used to implement the interpolator efficiently and no zero-stuffing was actually performed.

Due to the decimation by 10, the phase-locked loop runs at a sampling rate of 4800 Hz. Although the DPLL runs in scalar mode on the vector card, the lowered sampling rate sufficiently reduces its computational load that real-time operation can

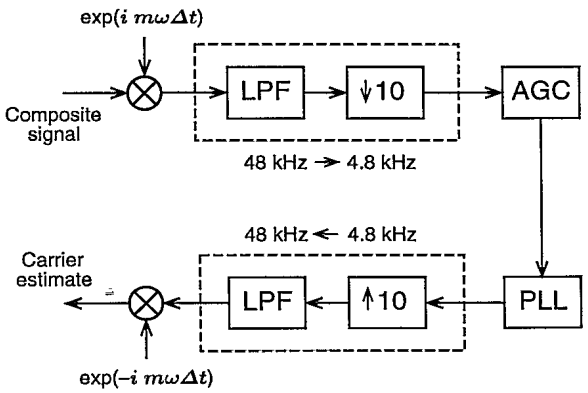

Figure 2. Generation of the local reference carrier.

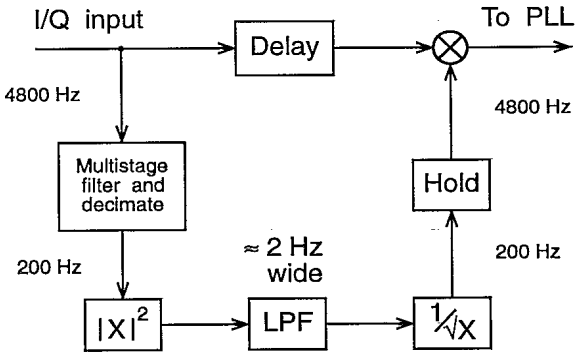

Figure 3. The automatic gain control (AGC).

be attained. (The DPLL accounts for approximately 33% of the computational load of the entire demultiplexer.)

B. *AUTOMATIC GAIN CONTROL*

The loop bandwidth of the DPLL depends on the amplitude of its input, and hence there must be a method for scaling the pilot to a known level. The AGC implemented here was based on the feedforward structure [3] shown in Fig. 3. The AGC computes the squared magnitude of the input signal, uses a lowpass filter to isolate the discrete component at DC, and scales the input accordingly.

The lowpass filter is quite narrow, on the order of several Hertz. Building such a narrow filter directly at the DPLL sampling rate of 4800 Hz would be difficult, and so several stages of filtering and decimation were introduced to get the sampling rate down to 200 Hz, a rate at which the desired narrow width can be attained without much trouble. The low sampling rate also reduces the computational load of the non-linear functions, such as the square root, to a negligible value.

Although the scaling factor is updated 200 times a second, the data to be scaled are still at the 4800-Hz sampling rate. The mismatch in sampling rate was handled by applying each scaling factor to $4800/200 = 24$ consecutive data samples (shown in

Fig. 3 as a hold operation.) The 200-Hz sampling rate is sufficiently high compared to the narrow filter width to ensure a smooth variation of the scale factor with time.

C. THE DIGITAL PHASE-LOCKED LOOP

A fairly extensive treatment of the DPLL design is now given. The theory of digital PLLs seems to be largely confined to the periodical literature [4, 5], whereas analog PLLs are treated in several textbooks [3, 6, 7]. Fortunately, much of the theory for the analog case carries over to the digital case.

C.1. The Non-Linear Model

A detailed schematic of the DPLL is given in Fig. 4. The loop filter consists of an integrator and a proportional path, with respective gains c_1 and c_2. The digitally controlled oscillator (DCO) consists of an integrator and a function generator that outputs the sine and cosine of the phase estimate $\hat{\theta}_n$. In practice it is necessary to continually reduce $\hat{\theta}_n$ modulo 2π to prevent it from growing without bound in the presence of a frequency offset (for which the phase is a ramp function), but this has been omitted for the purpose of analysis.

The DPLL contains two delay registers, which store the state variables $\hat{\theta}_n$ and y_n. Reading directly from Fig. 4, the state equations may be written down as

$$\hat{\theta}_{n+1} = \hat{\theta}_n + y_n + c_2 \sin\phi_n, \quad (1)$$

$$y_{n+1} = y_n + c_1 \sin\phi_n, \quad (2)$$

where $\phi_n \equiv \theta_n - \hat{\theta}_n$ is the phase error. An analytical solution of these non-linear difference equations does not appear possible. However, when the loop is locked and the phase error is small (e.g., $|\phi_n| < 30°$ or so), a linear model provides very accurate estimates of performance.

C.2. The Linear Model

The linear model for the DPLL is derived by using the small-angle approximation $\sin\phi_n \cong \phi_n$ in (1) and (2) to yield the equations

$$\hat{\theta}_{n+1} = \hat{\theta}_n + y_n + c_2\,\phi_n, \quad (3)$$

$$y_{n+1} = y_n + c_1\,\phi_n. \quad (4)$$

The advantage of the linear model is that transform techniques may be used in the analysis. In what follows, the z–transform of θ_n will be denoted by $\theta(z)$, and similarly for the other discrete-time variables. The closed-loop transfer function of the DPLL, defined by $H(z) \equiv \hat{\theta}(z)/\theta(z)$, is fundamental in determining the behavior of the loop. We find that

$$H(z) = \frac{c_2(z-1) + c_1}{(z-1)^2 + c_2(z-1) + c_1}, \quad (5)$$

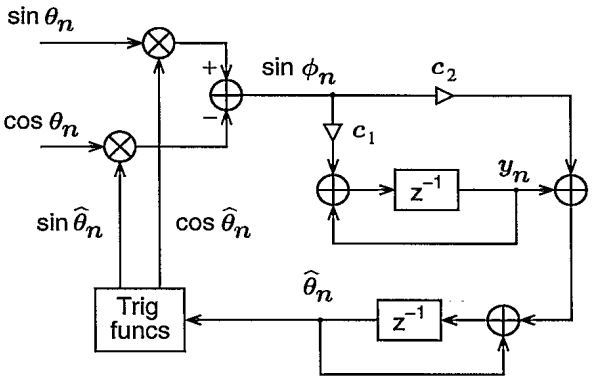

Figure 4. The digital phase-locked loop (DPLL). The output is $\exp(-i\,\hat{\theta}_n)$.

where $H(z)$ has been written in terms of $(z-1)$ for future convenience. The transfer function has two poles and thus the loop is classed as second-order.

The linear model can be used to evaluate the tracking performance of the loop. Of interest is the behavior of the phase error $\phi_n = \theta_n - \hat{\theta}_n$, which can be examined for large values of n using the final-value theorem of z–transform theory [8]. This theorem states that if ϕ_n attains a final value ϕ_∞ as $n \to \infty$, then

$$\phi_\infty = \lim_{z\to 1} \{\phi(z)(z-1)/z\}. \quad (6)$$

It is easily seen that ϕ_n has z–transform $\phi(z) = \big(1 - H(z)\big)\theta(z)$, and from (5) and (6) it follows that

$$\phi_\infty = \lim_{z\to 1} \left\{ \frac{(z-1)^3}{(z-1)^2 + c_2(z-1) + c_1} \frac{\theta(z)}{z} \right\}. \quad (7)$$

Of most interest is the final phase error for a frequency offset $\Delta\omega$, defined by

$$\theta_n = \begin{cases} 0 & \text{for } n < 0, \\ (\Delta\omega\Delta t)\, n & \text{for } n \geq 0, \end{cases} \quad (8)$$

where Δt is the sampling period. The corresponding z–transform is given by [8]

$$\theta(z) = \Delta\omega\Delta t\,[z/(z-1)^2]. \quad (9)$$

From (7) and (9) it follows that a frequency offset can be tracked by the second-order DPLL with no error. (The precise transient behavior depends on whether the loop remains in its linear regime; we are considering only the final phase error.)

C.3. Loop Filter Coefficients in Terms of Their Analog Equivalents

The theory of analog PLLs is well developed, and it is therefore convenient to relate the loop parameters of a digital PLL to their analog counterparts. The Laplace transform is used for the

analysis of analog filters, and we shall denote by s the transform variable. A second-order analog PLL with a perfect integrator has transfer function [3]

$$H_A(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{10}$$

where ζ is the damping coefficient and ω_n is the natural loop frequency. The damping coefficient is usually chosen to lie in the range $0.5 < \zeta < 2$.

The next step is to relate the parameters in (10) to the coefficients c_1 and c_2 in (5). To do this, we draw upon standard techniques for deriving digital filters from analog prototypes. The technique used here was based on keeping the impulse-response invariant [9]. Under the assumption that $\omega_n\Delta t \ll 1$, this procedure yields the approximate formulas

$$c_1 \cong (\omega_n\Delta t)^2 \quad \text{and} \quad c_2 \cong 2\zeta\omega_n\Delta t. \tag{11}$$

These results agree with those in [4].

C.4. The Effect of Noise

The above analysis shows that, in the absence of noise, the phase error is zero for a fixed frequency offset. However, as additive noise is also present at the input to the DPLL, the phase will be stochastically perturbed as a function of time. A complete analysis of the effect of noise in the nonlinear PLL is very difficult indeed. Fortunately, the SNR in our case is high enough to keep the loop in its linear regime while tracking, and a simple noise analysis suffices to derive the variance of the phase error. In the analog case, the phase error in the linear approximation is given by [3, 6]

$$\sigma_\phi^2 = N_o B_L / A^2, \tag{12}$$

where A is the RMS amplitude of the pilot (with units V), N_o is the power spectral density of the noise (V^2/Hz), and B_L is the one-sided noise bandwidth of the loop (Hz). This result also holds for the DPLL, assuming a perfect AGC. It remains only to compute the bandwidth B_L for the digital loop. It will now be shown that, to a good approximation, B_L for the DPLL is the same as for an analog PLL with transfer function (10).

The two-sided bandwidth of a digital filter with transfer function $H(z)$ is given by

$$B = \frac{1}{2\pi i}\int_C H(z)H(z^{-1})\frac{dz}{z}, \tag{13}$$

where C is the unit circle taken in the positive sense in the complex plane. Substituting $H(z)$ from (5) into (13) and using the residue calculus, it is found that the loop bandwidth of the DPLL is

$$B = \frac{c_1^2 + 2c_2^2 + 2c_1 - 3c_1c_2}{(c_2 - c_1)(c_1 - 2c_2 + 4)}. \tag{14}$$

We next substitute the formulas (11) into (14) and expand into a power series in $\omega_n\Delta t$. Again assuming that $\omega_n\Delta t \ll 1$ and retaining only the first term, we find that

$$B \cong \omega_n\Delta t\left(\zeta + \frac{1}{4\zeta}\right). \tag{15}$$

This is the two-sided bandwidth normalized to a 1-Hz sampling rate; in terms of actual frequency, the one-sided bandwidth of the digital loop is

$$B_L = \frac{B}{2\Delta t} \cong \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right). \tag{16}$$

The loop bandwidth of an analog PLL with transfer function (10) is given by this same formula [3, 6]. It should be noted that although ω_n has units of radians, (16) gives B_L in units of Hz.

C.5. Numerical Values of the Loop Filter Coefficients

In choosing numerical values for the coefficients c_1 and c_2, there are two opposing criteria to be considered. On the one hand, it is desired to make the loop bandwidth small in order to reduce the variance of the phase error [see (12)]. On the other hand, if the loop bandwidth is small compared to the frequency offset of the input, acquisition performance will suffer.

The sampling frequency at the input to the DPLL is 4800 Hz, so the sampling period is $\Delta t = 1/4800 = 2.08 \times 10^{-4}$ sec. The loop damping was set to $\zeta = 1/\sqrt{2} \cong 0.707$, a common choice. This leaves only the selection of $\omega_n = 2\pi f_n$ in order to define the loop coefficients via (11). Note that the choice of ω_n will also determine the loop bandwidth through (16). The value chosen was $f_n = 15$ Hz, which yields a bandwidth $B_L = 50$ Hz. As the maximum allowed frequency offset of the pilot is ± 25 Hz, a 50-Hz loop bandwidth should ensure good acquisition, as will be verified below. The filter coefficients are then determined from (11) to be

$$c_1 = 3.8553 \times 10^{-4} \quad \text{and} \quad c_2 = 2.7768 \times 10^{-2}.$$

Note that $\omega_n\Delta t = 1.96 \times 10^{-2} \ll 1$, as was assumed in the previous derivations. Given the numerical values of A and N_o the phase variance can be computed via (12), but this calculation is omitted here.

C.6. Acquisition

At system start-up, the DPLL must acquire, or lock onto, the input signal. Because the allowed frequency offset of ± 25 Hz is small compared to the 7500-Hz center frequency ($< 1\%$), it was decided to use natural, or unaided, acquisition. The initial errors in the DPLL state variables may be

quite large, and so non-linear analysis must be used in studying acquisition.

First, the state equations (1) and (2) may be re-written in the form

$$\phi_{n+1} = \phi_n - y_n - c_2 \sin\phi_n + (\theta_{n+1} - \theta_n), \quad (17)$$
$$y_{n+1} = y_n + c_1 \sin\phi_n, \quad (18)$$

where now the phase error $\phi_n = \theta_n - \hat{\theta}_n$ is taken as one of the update variables. The term $(\theta_{n+1} - \theta_n)$ is the digital instantaneous frequency and can be considered the input, or forcing function, in the above equations. The input of most interest for investigating acquisition behavior is a fixed frequency offset, for which $\theta_n = (\Delta\omega\Delta t)\, n$. Then the instantaneous frequency is just $\Delta\omega\Delta t$, and the state equations become

$$\phi_{n+1} = \phi_n - e_n - c_2 \sin\phi_n, \quad (19)$$
$$e_{n+1} = e_n + c_1 \sin\phi_n, \quad (20)$$

with $e_n \equiv y_n - \Delta\omega\Delta t$. The variables ϕ_n and e_n are measures of the phase and frequency errors respectively.

Figure 5 shows a phase-plane plot, which graphically represents the numerical solutions of the state equations. Each line traces out the locus of a point (ϕ_n, e_n) as n increases, the direction being indicated by an arrow. The equilibrium position is at the origin, where the errors are zero. Although the phase error can assume any real value, the phase plane plot is 2π-periodic in ϕ_n, and only one period is shown.

Figure 5 is based on the numerical values of c_1 and c_2 given above. The maximum frequency offset allowed in the 7.5-kHz pilot is ± 25 Hz, and it is seen from the figure that the DPLL will easily acquire the pilot. In the area between the thick lines (the so-called separatrices), the DPLL settles to the equilibrium point at the center of the plot, while for other inputs the DPLL skips cycles; i.e., the phase passes through the left or right edge of the plot, and the loop eventually settles at an equilibrium point some multiple of 2π away. For a frequency offset of ± 25 Hz the loop will skip at most one cycle.

IV. SUMMARY

The implementation of a digital phase-locked loop has been described for a demultiplexer application in which a pilot tone must be isolated at the receiver. It was shown that the DPLL and its associated AGC can be implemented at baseband by placing them between a quadrature demodulator and a remodulator; sampling rate conversions can then be exploited to gain computational efficiency.

REFERENCES

[1] H. Taub and D.L. Schilling, *Principles of Communication Systems.* New York: McGraw-Hill, 1971.

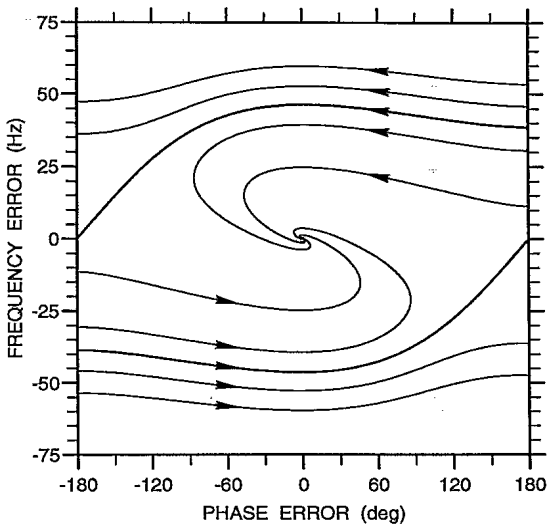

Figure 5. Phase-plane plot of the DPLL response.

[2] D.C. Rife and R.R. Boorstyn, "Single-tone parameter estimation from discrete-time observations," IEEE Trans. Info. Theory, vol. 20, pp. 591–598, September 1974.

[3] H. Meyr and G. Ascheid, *Synchronization in Digital Communications*, Vol. 1. New York: John Wiley, 1990.

[4] Y.R. Shayan and T. Le-Ngoc, "All digital phase-locked loop: concepts, design and applications," IEE Proceedings, vol. 136, Pt. F, pp. 53–56, February 1989.

[5] J. Garodnick, J. Greco, and D.L. Schilling, "Response of an all digital phase-locked loop," IEEE Trans. on Communications, vol. 22, pp. 751–764, June 1974.

[6] A.J. Viterbi, *Principles of Coherent Communication.* New York: McGraw-Hill, 1966.

[7] F.M. Gardner, *Phaselock Techniques*, 2nd ed. New York: John Wiley, 1979.

[8] D.J. DeFatta, J.G. Lucas, and W.S. Hodgkiss, *Digital Signal Processing: A System Design Approach*, John Wiley and Sons, 1988. (pp. 90–91).

[9] A.V. Oppenheim and R.W. Schafer, *Digital Signal Processing.* Englewood Cliffs, NJ: Prentice-Hall, 1975.

#506667