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DESIGN AND PERFORMANCE OF A HIGH DYNAMIC RANGE CLAMPING AMPLIFIER FOR A MAWS TRANSCEIVER

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by

D. Michael Bowry and Bob W. Robinson

DEFENCE RESEARCH ESTABLISHMENT OTTAWA

TECHNICAL NOTE 96-006

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ABSTRACT

The Defence Research Establishment Ottawa (DREO) has been conducting research and development activities in the field of active missile approach warning systems (MAWS) to support the CF-18 MAWS requirement. A MAWS transceiver and a controller/data acquisition system (C/DAQU) were developed by DREO for use in flight trials. To avoid the long recovery time involved with hard saturation of the analog-to-digital converter in the C/DAQU, a clamping amplifier is required for the last stage in the receive chain of the transceiver. Because no off-the-shelf product was available that would meet the stringent requirements of this application, a clamping amplifier was developed, fabricated, and tested at DREO using in-house laboratory equipment. This technical note outlines the design specifications, the performance issues (dynamic range, third order intermodulation products, and saturation recovery time), and the performance results of the clamping amplifier.

RESUME

Le Centre des recherches pour la défense d'Ottawa (CRDO) mène des activités de recherche et développement dans le domaine des systèmes actifs d'avertisseur d'approche de missiles (MAWS) pour être en mesure de soutenir les exigences MAWS du CF-18. Nous avons mis au point un émetteur-récepteur MAWS et une unité de commande du système d'acquisition de données (C/DAQU) destinés aux essais en vol. L'étage d'amplification de la chaîne de réception de l'émetteur-récepteur requiert un amplificateur restrictif pour éviter les trop longs temps de récupération lors de la saturation brusque du convertisseur analogique numérique du C/DAQU. Vu qu'aucun produit respectant les exigences rigoureuses de cette application n'était sur le marché, nous avons dû concevoir, fabriquer et mettre à l'essai notre propre amplificateur restrictif dans les laboratoires du CRDO. Cette note technique expose les grandes lignes des caractéristiques, des problèmes de performance (c'est-à-dire la dynamique de mesure et les produits d'intermodulation de troisième ordre, le temps de récupération lors de la saturation), ainsi que des résultats de performance de l'amplificateur restrictif.

EXECUTIVE SUMMARY

The Defence Research Establishment Ottawa (DREO) has been conducting research and development activities in the field of active missile approach warning systems (MAWS) to support the CF-18 MAWS requirement. A MAWS transceiver and a controller/data acquisition system (C/DAQU) were developed by DREO for use in flight trials. The last stage of the receive chain in the transceiver down-converts the radar return to an intermediate frequency, which is then digitized by a 10 MHz, 14 bit analog-to-digital converter (ADC). The last stage must also provide amplification to that return, while clamping the output to a desired threshold so as to restrict the degree of potential ADC saturation. ADC saturation is possible with the MAWS transceiver during strong radar returns in low level flight. While the ADC is saturated, analog-to-digital conversion will output its full scale, digitized value, and can no longer follow the voltage changes at its input. When the signal level falls below full scale, there is an inherent recovery time which is proportional to the degree of saturation. The clamping amplifier presented in this technical note prevents hard saturation by preventing the output from exceeding a specified threshold voltage, thereby minimizing the recovery time.

To meet the MAWS transceiver design specifications, the amplifier must be able to recover from saturation in 50 ns or less. It must also provide at least 73 dB of dynamic range when the amplifier output is below the clamping threshold (normal operation). Because no off-the-shelf product was available that would meet the stringent requirements of this application, a clamping amplifier was developed, fabricated, and tested at DREO using in-house laboratory equipment. The performance tests demonstrated that the amplifier design exceeds the dynamic range requirement. The recovery time requirement was met by setting the clamping threshold to a level that would limit the ADC recovery time to approximately 50 ns after saturation had subsided. This recovery period results in a maximum loss of only one valid sample of data. This technical note outlines the design specifications, the performance issues (dynamic range, third order intermodulation products, and saturation recovery time), and the performance results of the clamping amplifier.

CONTENTS

1.0 INTRODUCTION

The Defence Research Establishment Ottawa (DREO) has been conducting research and development activities in the field of active missile approach warning systems (MAWS) to support the CF-18 MAWS requirement. A MAWS transceiver and a controller/data acquisition system (C/DAQU) were developed by DREO for use in flight trials. An active MAWS uses a pulse Doppler radar to detect incoming missiles with enough warning time to allow the deployment of countermeasures. Installed on the CF-18 is a radar warning receiver capable of detecting incoming radar guided missiles by detecting the missile's tracking radar emissions. The CF-18 is vulnerable, however, to heat-seeking missiles which passively home in on the aircraft's infrared signature.

The DREO MAWS transceiver transmits RF pulses at a specified pulse repetition frequency. Between transmitted pulses, the controller/data acquisition system (C/DAQU) collects radar returns and stores the raw data digitally for further processing. The AMP17 block contains the last amplifier stage in the receive chain before the input to the Echotek ETAD14 10 MHz 14 bit analog-to-digital converter (ADC). This ADC board uses the Analog Devices AD9014 chip to perform the conversion. An input voltage greater than ±1 V, will saturate the ADC. During this condition, the ADC output can no longer follow changes on its input, and will simply output its maximum value. Without clamping or limiting of the amplifier output, the ADC can become "hard" saturated. Hard saturation results in excessive recovery time and subsequent loss of data.

Because no off-the-shelf product was available that would meet the stringent requirements of this application, a clamping amplifier was developed, fabricated, and tested at DREO using in-house laboratory equipment. Chapter 2 outlines the design specifications, including power output, clamping threshold, and dynamic range. Chapter 3 discusses the design and various concerns that will affect the amplifier's performance. Chapter 4 outlines the test setup used and provides results from performance tests in the form of frequency spectrum plots. Chapter 5 summarizes the results and compares the success of the design to the original specifications.

2.0 DESIGN SPECIFICATIONS

The input of the ADC will accept levels between ±1 V. The input impedance is 50Ω. As demonstrated in Equations 2-1 and 2-2, this gives a maximum ADC input power of 10 mW or 10 dBm.

$$V_{in,rms} = \frac{1\ V_{pk}}{\sqrt{2}} = 0.707\ V \tag{2-1}$$

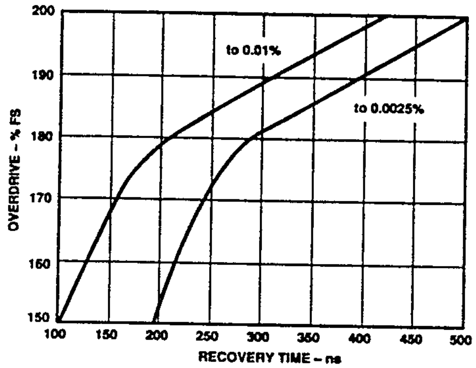
$$P_{in} = \frac{(0.707\ V)^2}{50\ \Omega} = 10\ mW = +10\ \text{dBm} \tag{2-2}$$

The final amplifier stage must be able to supply at least 20 mA of output current to the 50 Ω ADC input.

$$\frac{1\ \text{V}pk}{50\ \Omega} = 20\ mA \tag{2-3}$$

The ADC outputs a 14 bit word giving 16384 quantization levels. This would give the ADC an ideal dynamic range of 84.29 dB. The best dynamic range achieved by Echotek, sampling at 10 MHz, was 72.84 dB [1]. MPB Technologies was able to achieve a dynamic range of 68.33 dB in the same test [1]. Based on the best performance achieved with the Echotek board, the clamping amplifier was required to have 73 dB of dynamic range when the output of each individual tone (during a two-tone test) was +4 dBm. Here, dynamic range is defined as the power difference between the maximum single output tone and the strongest unwanted signal (noise, harmonic distortion, or intermodulation products) within the operating bandwidth.

The ADC samples data at a rate of 10 MHz or once every 100 ns. Figure 2-1 shows the percentage overdrive (saturation) vs. the recovery time of the ADC [3]. To minimize the number of saturated data samples, the clamping amplifier is required to limit the signal level so that the ADC can recover in 50 ns. Figure 2-1 gives recovery times down to only 150% overdrive. Assuming that the graph continues to be linear below 150% overdrive, 130% overdrive should result in a recovery time of 50 ns. The clamping threshold is therefore set to ±1.3 V.



Overvoltage Recovery Time

Figure 2-1. Percentage Overdrive vs. Recovery Time for the AD9014

Figure 2-2 is a diagram of the functional requirements of the AMP17 block. The mixer is the final down-converting stage for the receive chain, and is required to convert the RF signal to an IF frequency of 2.5 MHz. Target returns arriving at the antenna are extremely weak. The receive chain in the MAWS transceiver was designed to provide as much gain as possible to the target return, while still preventing (in most instances) saturation of the ADC due to clutter. To achieve the required gain in the receive chain, the final amplifier is required to provide 28 dB of gain. The amplifier must also clamp the output during saturation conditions.

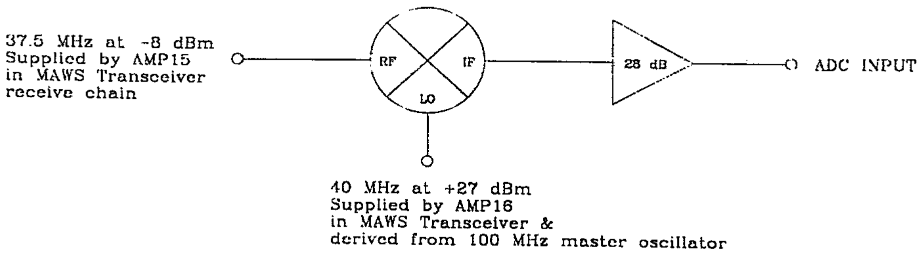


Figure 2-2. Functional Diagram for AMP17

3.0 THE DESIGN

3.1 THIRD ORDER INTERMODULATION PRODUCTS

Intermodulation products are generated by non-linearities inherent to the device under test (DUT). When two signals of different frequency are input to the DUT, its non-linearities cause the two tones to beat against each other. The frequency difference is called the beat frequency. As a result, intermodulation tones will appear at ± *m*f1 ± *n*f2; where f1 and f2 are the frequencies of the desired tones and *m* and *n* are integers greater than zero. The summation *m* + *n* indicates the order of the intermodulation product. Third order intermodulation products or "intermods" are the most troublesome for the designer because they are the strongest. Also, they appear at 2f1 - f2 and 2f2 - f1, only a single beat frequency away from the desired tone. The intermods appearing at 2f1 + f2 and f1 + 2f2 appear outside the system bandwidth and are of no concern. For the purpose of this technical note, the term "intermod" will refer only to third order intermodulation products and will be the figure of merit for dynamic range.

Greater non-linearities will result in stronger intermods. The level of intermod power is dependent on the output power of the DUT. When the DUT is forced to output more power, the intermods will increase. This increase in intermod power is three times that of the output power increase (3-to-1 rule). For example, increasing the output power of each tone in the DUT by 10 dB will force the intermods up by 30 dB. The loss in dynamic range is the difference or 20 dB. The reverse is also true. A decrease in output of 10 dB will lower the intermods by 30 dB giving a dynamic range improvement of 20 dB.

A device is characterized for intermod performance by its third order intercept point or IP3. IP3 is the point at which the intermod power is equal to the output power of the desired signal. From this point, the designer can extrapolate back to the desired output power and predict the resulting intermod power. It should be pointed out that the IP3 is a theoretical value which is derived from measurements in the operating region. The device would normally be destroyed before reaching the IP3. Figure 3-1 illustrates the above discussion.

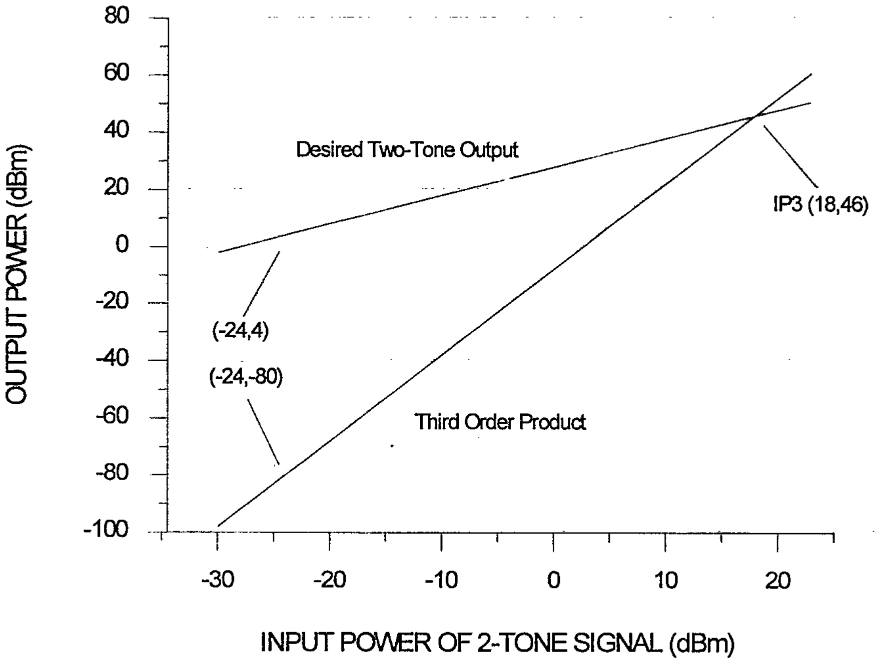


Figure 3-1. Relationship between Output Power of DUT and Intermods

As seen in Figure 3-1, the importance of a high IP3 is obvious. A higher IP3 will produce lower intermods at any given input power, and will therefore contribute to a higher dynamic range. In the two tone scenario, intermods will appear in the frequency spectrum, offset from the desired tones by the beat frequency. As a result, intermods will often appear within the system bandwidth and therefore cannot be eliminated by filters. Intermodulation products also use up the available signal power leaving less for the desired signals. If the intermod products are not minimized, the desired signals could be forced below the detection threshold. With the proper choice of amplifier, the intermods can be kept low enough (73 dB below the maximum desired signal) to meet the dynamic range requirements. The AD8036 clamp amp was chosen as the final stage of amplification in IFAMP17. Its IP3 is +46 dBm and its theoretical intermod performance is shown in Figure 3-1.

Another design consideration for intermod performance is the amplifier's maximum output current. As an amplifier is driven harder, its non-linearities will increase. It is therefore important to choose a device that greatly exceeds the current requirement. The AD8036 satisfies this condition. The AD8036 clamping amplifier is able to source 70 mA. The amplifier design requires 20 mA or 29 percent of the AD8036's maximum.

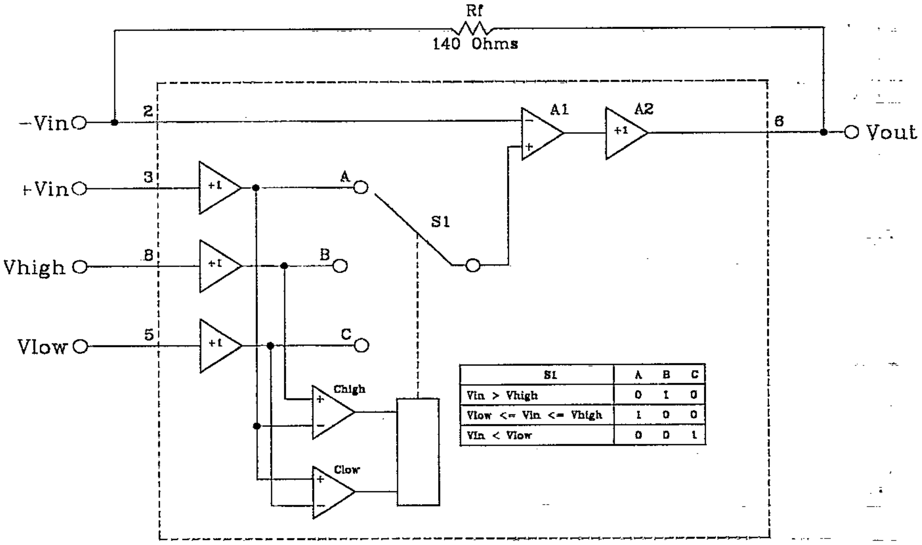
3.2 LIMITING OF THE OUTPUT

Depicted below in Figure 3-2 is a simplified block diagram of the AD8036 when operated in the non-inverting configuration with unity gain [2]. $+V_{IN}$ is compared to V_{HIGH} and V_{LOW} by the C$_{HIGH}$ and C$_{LOW}$ comparators respectively. V_{HIGH} and V_{LOW} are shown in Equations 3-1 and 3-2:

$$V_{HIGH} = \frac{V_{CH}}{G} \tag{3-1}$$

$$V_{LOW} = \frac{V_{CL}}{G} \tag{3-2}$$

where V_{HIGH} is the high input clamping level, V_{LOW} is the low input clamping level, V_{CH} is the high output threshold, V_{CL} is the low output threshold, and G is the closed loop gain of the AD8036. Following the truth table for switch S1: if $+V_{IN}$ is less than V_{HIGH} and greater than V_{LOW}, then the switch goes to position A and $+V_{IN}$ is connected to the non-inverting input of the differential to single-ended amplifier, A1. This represents operation in the non-clamping region, and the AD8036 behaves like a traditional op-amp.



S1	A	B	C
Vin > Vhigh	0	1	0
Vlow <= Vin <= Vhigh	1	0	0
Vin < Vlow	0	0	1

Figure 3-2. Block Diagram of AD8036 Clamping Op-Amp

If $+V_{IN}$ is greater than V_{HIGH} , then S1 goes to position B, and V_{HIGH} is connected to A1. As long as this condition continues, V_{OUT} will stay at V_{CH} (V_{HIGH} times the closed-loop gain of the op-amp). If $+V_{IN}$ is less than V_{LOW}, then S1 goes to position C and V_{LOW} is connected to A1. While this is true, V_{LOW} will stay at V_{CL} (V_{LOW} times the closed-loop gain). The worst case error of the clamping action is typically 18 mV times the closed loop gain occurring when $+V_{IN}$ equals V_{HIGH} or V_{LOW}. This will settle to within 5mV of the ideal as $+V_{IN}$ passes either V_{HIGH} or V_{LOW}. When the AD8036 output returns to the linear, non-clamped region of operation, it will experience an inherent recovery time. The AD8036 data sheet quotes a 1.5 ns recovery period for a X2 overdrive condition, e.g. ±2.6 V at the output. Under most normal operating conditions, this overdrive condition is not exceeded.

3.3 THE SCHEMATICS

The mixer and amplifier portions of the AMP17 design have been split into two separate blocks. Each block is packaged in its own enclosure. The first block is called RFAMP17, and is displayed in Figure 3-3. The output of RFAMP17 is connected to a low pass filter (LPF) with a corner frequency of 3.5 MHz. The output of the 3.5 MHz LPF is connected to the amplifier input in the IFAMP17 block displayed in Figure 3-4. In RFAMP17, the radar return is mixed down from 37.5 MHz to 2.5 MHz. The IF output is then attenuated by 3 dB and put through a 5 MHz LPF (PLP 5). The 3 dB attenuator improves the impedance match between the mixer and the LPF. The LO to IF isolation for U1 is only 40 dB, and the RF to IF isolation is 25 dB. The LPF provides further attenuation of at least 40 dB to the undesired 37.5 MHz and 40 MHz signals that find themselves at the mixer output, IF. As mentioned in the intermod discussion above, as an amplifier is driven harder, its inherent non-linearities will increase, and therefore intermod performance will decrease. The 37.5 MHz and 40 MHz signals are not desired at the output, and the presence of these signals will only increase intermods. These signals are thus filtered out.

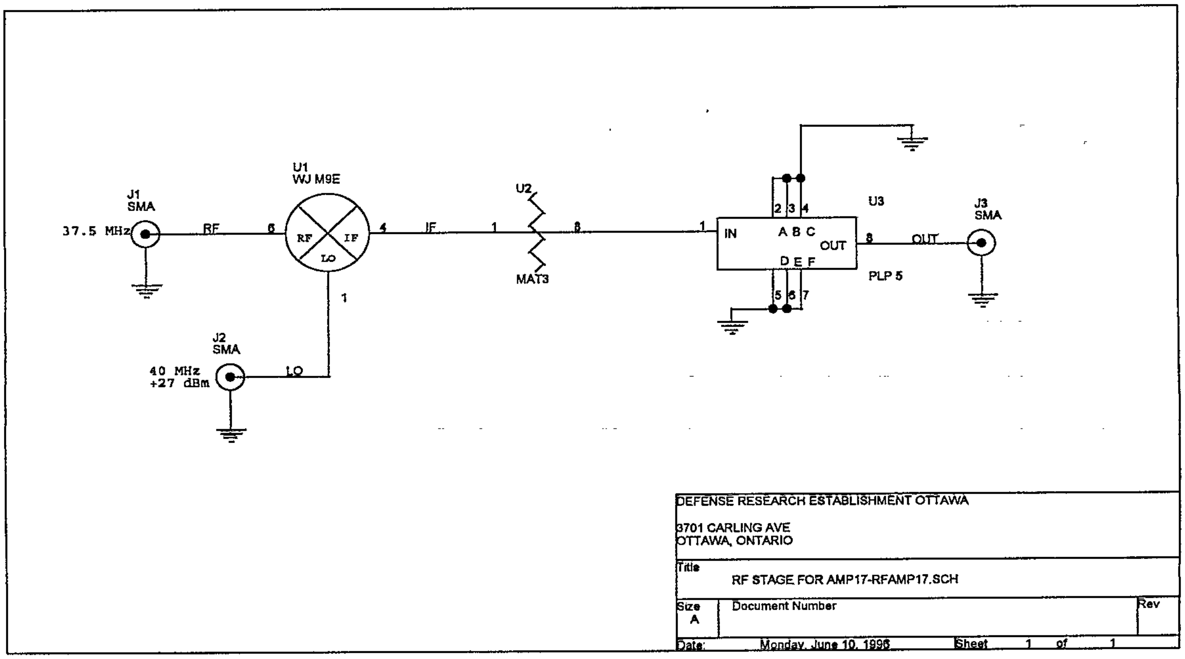


Figure 3-3. Schematic of RFAMP17

The final block of AMP17 is IFAMP17. It contains two stages of gain (22 dB and 6 dB). The 22dB stage nulls out any DC output offset voltage. The 6 dB stage provides the clamping function. Please refer to Figure 3-4 below for the schematic. The high and low clamp inputs are configured so that the output will fully clamp at ±1.3 V. It is a characteristic of the AD8036 to begin clamping at approximately 80 percent of the clamp threshold. In this case the AD8036 will begin clamping just above ±1 V. After this point the device becomes highly non-linear and the resulting intermods increase at a rate higher than the 3-to-1 rule. This result is of no concern because the ADC saturates at ±1 V and the resulting data no longer follows the input. A level of ±1.3 V does not force the ADC into hard saturation and is not detrimental to ADC performance. As discussed in Chapter 2, 130 percent overdrive of the ADC input will result in a 50 ns recovery time after the overdrive (saturation) condition is relieved. This results in one valid data sample being lost, which is acceptable.

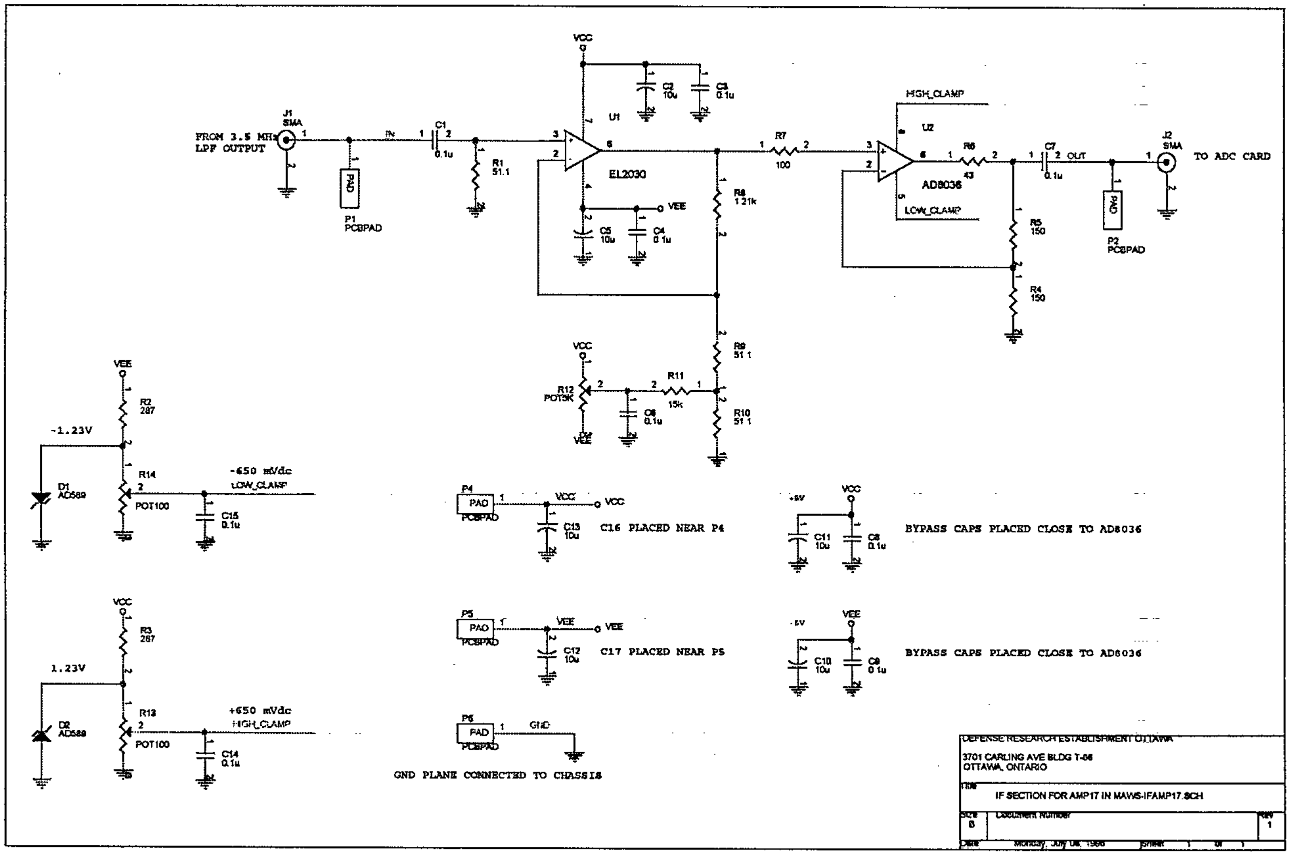


Figure 3-4. Schematic of IFAMP17

Depicted below in Figure 3-5 is the AMP17 integration plan for the MAWS transceiver. All module connections are of 50 Ω semi-rigid cable terminated in male SMA connectors providing a 100 percent shield ground. Originally, the RFAMP17 and IFAMP17 circuits were placed on the same printed circuit board (PCB). In this configuration, it was found that the LO was bypassing the 5 MHz LPF and reaching the 22 dB amplifier input. This drove the amplifiers harder than necessary, and increased their non-linearities. Intermod performance decreased. It was theorized that the LO trace was coupling onto the output trace of the 5 MHz LPF.

To correct this condition, RFAMP17 was given its own PCB and enclosure. When designing the PCB layout for RFAMP17, the LO trace was kept away from the LPF output as far as practically possible to avoid coupling. The centre conductor and shield ground of the SMA bulkhead feed-thru jacks were soldered directly to the PCB to improve grounding and the input/output signal connections. With these improvements, an LO to OUT isolation of 103 dB was achieved. This 103 dB is comprised of the 40 dB of LO to IF isolation from the mixer (WJ M9E) and 63 dB of attenuation from the 5 MHz LPF (PLP 5). The RF to OUT isolation was 77.8 dB.

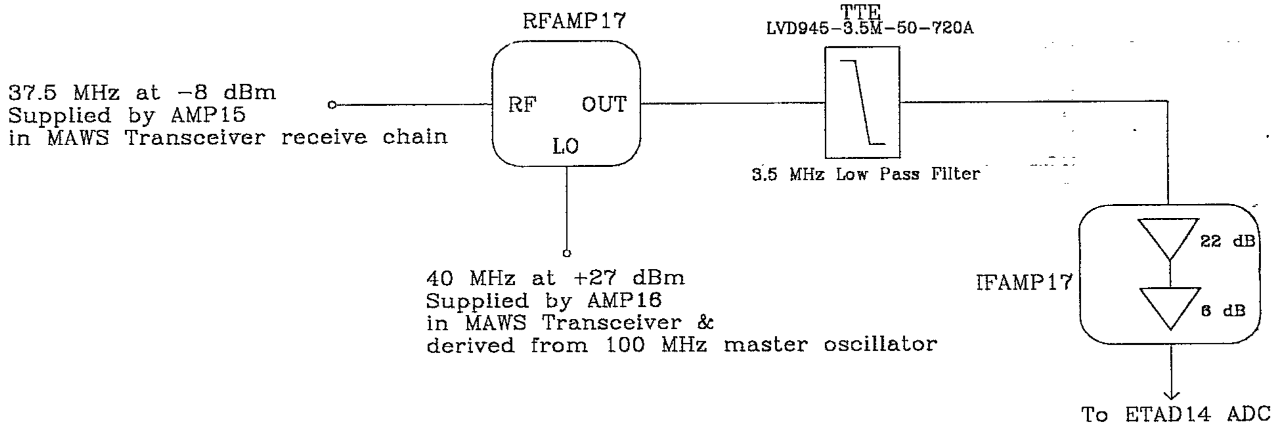


Figure 3-5. AMP17 Integration into MAWS Transceiver

4.0 RESULTS OF PERFORMANCE TEST

To test the performance of AMP17, two tones of 37.5 MHz and 37.514 MHz are combined and input into RFAMP17 where they are mixed down to 2.5 MHz and 2.486 MHz. The difference frequency of 14 kHz results in two intermods at 2.472 MHz and 2.514 MHz which fall in the 2 MHz 3 dB bandwidth of the receive chain. Figure 4-1 shows the equipment setup used to assess the performance of AMP17. All connections between modules are made with 50 Ω semi-rigid cable terminated with a male SMA connector on each end. The custom 20 dB amplifier module is the first prototype of the IFAMP17 design. The first stage of the circuit is identical to the first stage of what is now IFAMP17 except the gain is 20 dB instead of 22 dB. This additional amplifier was included because the signal generator/combiner circuit did not have sufficient intermod performance to handle the proper power requirement. To exercise the clamping amplifier at the proper input power the custom amplifier was introduced at the IFAMP17 input. This allowed a reduction in the output power of the signal generators by 20 dB and lowered the signal generator/combiner intermods to acceptable levels.

To set up equal power levels for the two-tone test, the HP8660C was set to its lowest power setting effectively eliminating it from the output frequency spectrum. The Marconi 2041 was then increased in power until the spectrum analyzer showed a +4 dBm power level. Note that +4 dBm from each tone produces a maximum output of +10 dBm. In the time domain, the two tones constructively and destructively interfere with each other. At times of 100 percent constructive interference, the output voltage is effectively doubled. This adds $20\log 2 = 6\,\mathrm{dB}$ of power to the output, and therefore presents +10 dBm of power to the ADC input. With this done, the output power of the HP8660C was increased to match the level of the Marconi 2041. The digital readout for the Marconi showed -21.3 dBm, and this is shown for both generators in Figure 4-1.

The data displayed on the spectrum analyzer was collected via an IEEE488 to PC Parallel Port interface module and stored on an AST PowerExec EL laptop computer. The computer used a program to control the download of output data from the spectrum analyzer to the laptop hard drive.

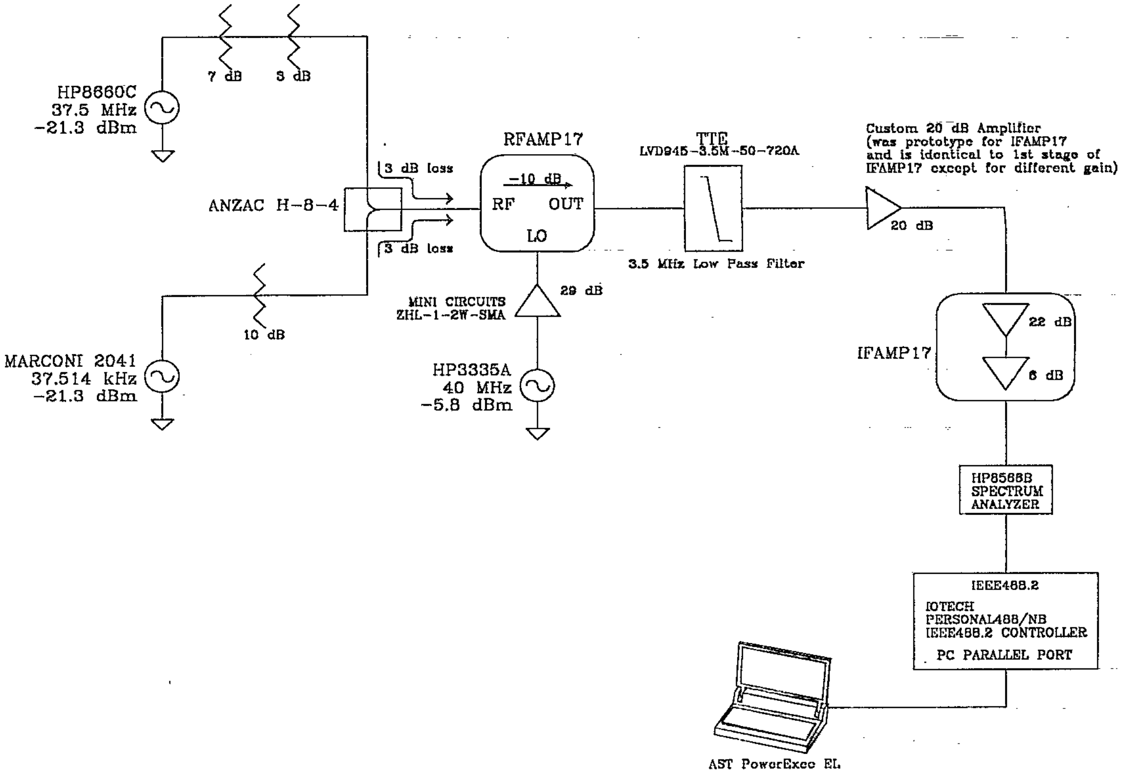


Figure 4-1. Equipment Setup for AMP17 Performance Test

With a frequency span of 50 kHz and a centre frequency of 2.493 MHz, Figure 4-2 shows the result of the above two tone test. Note the intermod at 2.472 MHz. In this plot the intermod is 73.9 dB down from the 2.486 MHz tone and represents the dynamic range of the AMP17 design. It should be noted that all quoted data coordinates used in figures depicting frequency spectra come from the raw data downloaded from the spectrum analyzer via the IEEE488 interface. The number of significant figures in the output power level are the result of a microprocessor output and are not realistic due to the inherent inaccuracy of the spectrum analyzer. Amplitude measurements should be considered accurate to the nearest dB. Frequency accuracy is largely dependent on frequency span as explained below.

Figure 4-3 shows the same output signal but with a 1 MHz span and the same centre frequency. Excluding spurious frequency spikes, the noise floor is shown to be 76 dB down from the desired two signal tones.

Harmonic distortion for AMP17 is displayed out to 100 MHz in Figure 4-4. From this it can be seen that the second harmonic is 53.8 dB down from the 2.5 MHz fundamental. All other harmonics below 100 MHz are below the noise floor. The spike shown at 13.659 MHz is not a harmonic or an intermodulation product. One possibility is that it could be appearing due to pick up from the outside environment. This second harmonic and spike are eliminated with the LPF which is installed at the input to the AD9014 ADC [1]. This device is a Mini-Circuits 5 MHz LPF.

The discrepancies in the frequency coordinate points are due to the resolution of the spectrum analyzer. For example, (2.5824 , 3.7) shown in Figure 4-4 should actually have a tone at 2.486 MHz and 2.5 MHz as indicated in Figure 4-2. The spectrum analyzer is sweeping across 99 MHz with only 1000 points to display the information for the harmonic plot (Figure 4-4). In this plot, each frequency coordinate is successively greater by 98.9 kHz. The 2.486 MHz and 2.5 MHz tones both fall into the frequency bin starting at 2.4835 MHz and stopping at 2.5824 MHz.

The spike at 5.1538 MHz shown in Figure 4-4 is an exception to this rule but can be explained. Once the start and stop frequencies are set, the frequency coordinate for each point on the display is determined by a programmed algorithm. For example, when sweeping from 1 MHz to 100 MHz, the tenth display point will always be at 1.8901 MHz. Now, ideally the sweep oscillator connected to the LO input of the front end mixer sweeps across the frequency span at a constant, linear rate. As a result, the harmonic at 5 MHz will fall into the frequency bin starting at 4.956 MHz and stopping at 5.0549 MHz. The display will show a tone at 5.0549 MHz. Realistically, the sweep oscillator has inherent non-linearities and will not traverse the frequency span at a constant rate, e.g. dfreq/dt is not a constant, but a function of time. When the ADC in the spectrum analyzer digitizes the amplitude for the 5.0549 MHz data point, the sweep oscillator finds itself in the next frequency bin, 5.0549 MHz to 5.1538 MHz. The 5 MHz harmonic is now shown as 5.1538 MHz with a power of -50.1 dBm.

These sources of error decrease with the increased resolution of a narrower frequency span. The intermod plot (Figure 4-2) spans 50 kHz over 1000 points, giving a resolution of 50 Hz per point. The dfreq/dt non-linearity is much smaller and therefore provides a picture much more realistic than the harmonic plot (Figure 4-4).

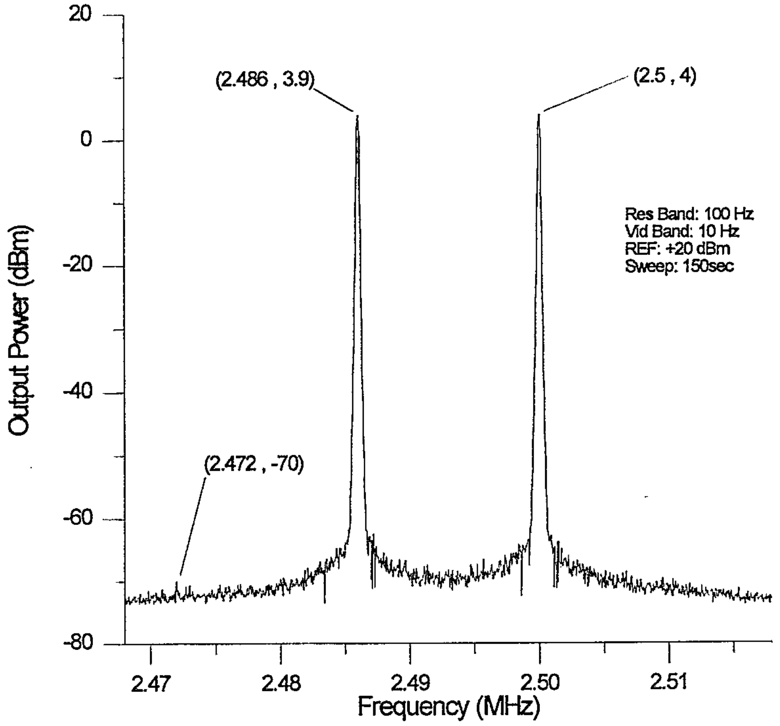


Figure 4-2. Frequency Spectrum of IFAMP17 Output Showing Intermod

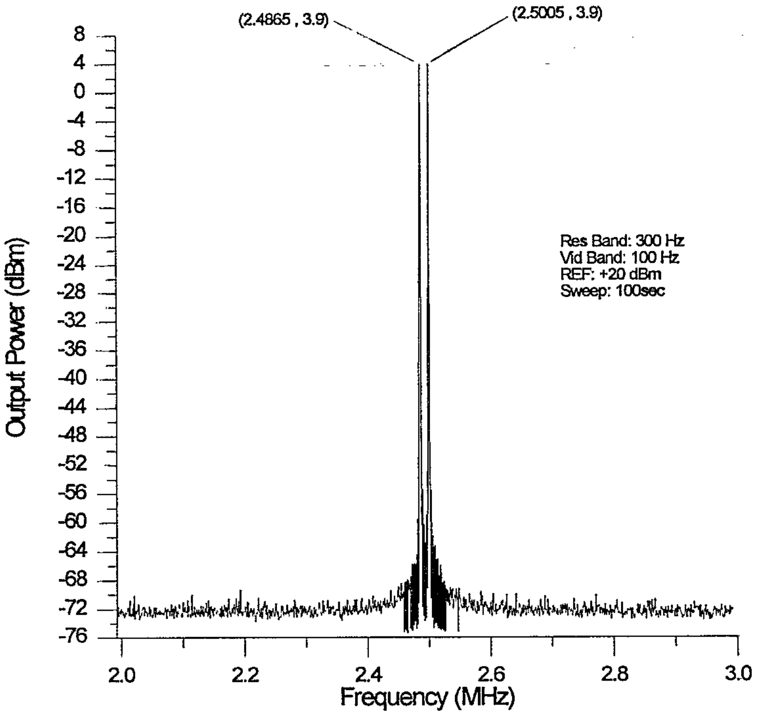


Figure 4-3. Noise Floor Plot of IFAMP17 Output

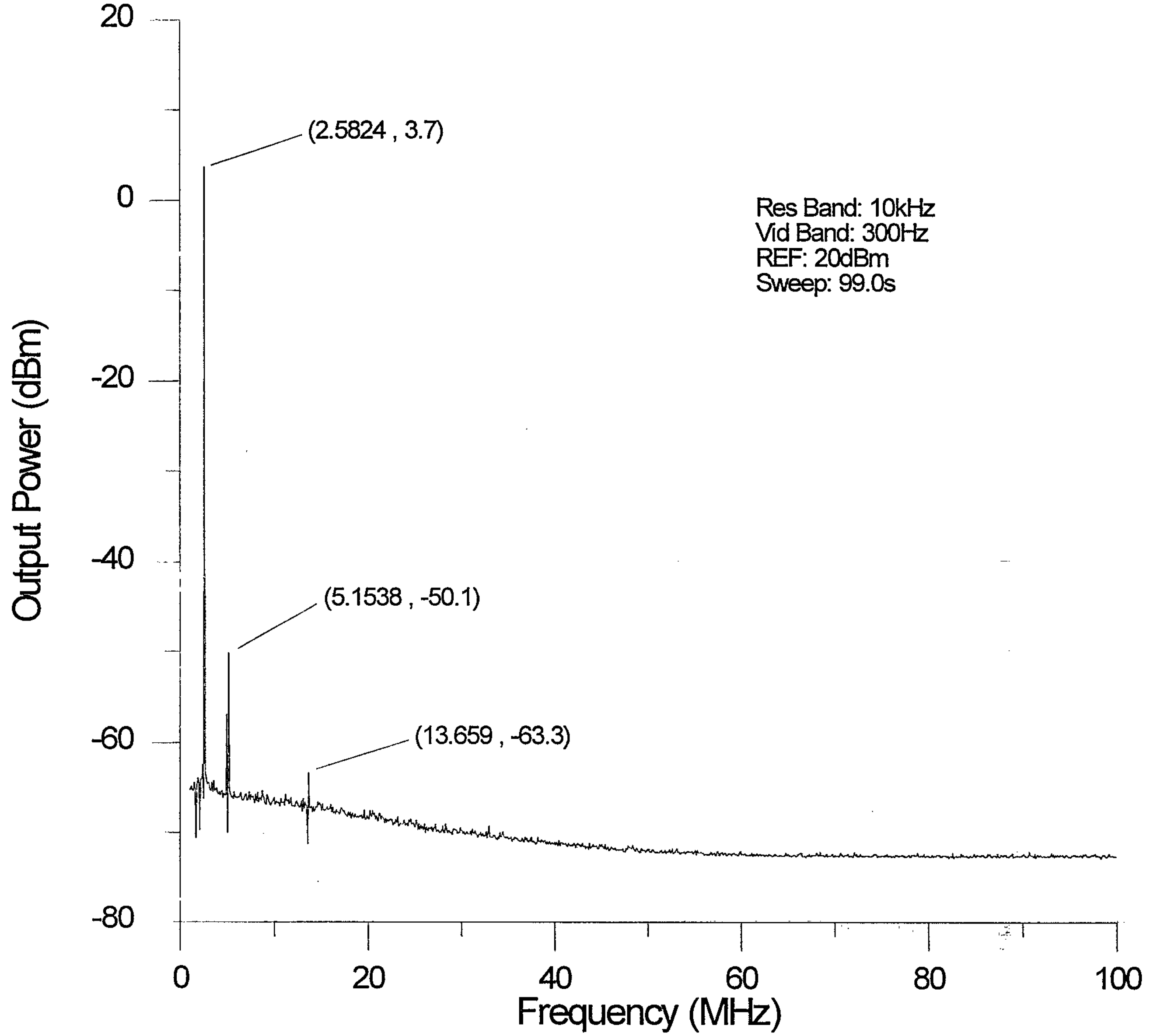


Figure 4-4. Harmonic Distortion of IFAMP17 Output

5.0 SUMMARY

The two measures of performance for the clamping amplifier design are dynamic range and necessary recovery time for the ADC after saturation is relieved. The maximum level of harmonic distortion was never given a concrete specification since the ADC is lowpass filtered and all harmonics are attenuated to levels below the resolution of the ADC.

The best signal-to-noise ratio (SNR) or dynamic range achieved for the ADC was measured by Echotek as 72.84 dB. MPB Technologies achieved a SNR of only 68.33 dB. The plot in Figure 4-2 shows a dynamic range of 73.9 dB for IFAMP17, which exceeds the design requirements. The intermods of the clamping amplifier are, therefore, unobservable by the ADC.

The clamping output threshold of ±1.3 V has been determined to be the optimum setting for acceptable ADC recovery time. With this setting, clamping does not start until ±1V and the calculated recovery time is limited to 50 ns. This will result in only one valid sample being lost after the ADC input comes out of saturation.

6.0 REFERENCES

[1] Nguyen, P., "ETAD14 and FIFO/RAM Evaluation Report", MPB Technologies, Pointe Claire, Quebec, 1994.

[2] "Low Distortion, Wide Bandwidth Voltage Feedback Clamp Amps AD8036/AD8037", Analog Devices Inc., Norwood, MA, USA, 1994.

[3] "14-Bit, 10 MSPS A/D Converter", Analog Devices Inc., Norwood, MA, USA, 1992.

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The Defence Research Establishment Ottawa (DREO) has been conducting research and development activities in the field of active missile approach warning systems (MAWS) to support the CF-18 MAWS requirement. A MAWS transceiver and a controller/data acquisition system (C/DAQU) were developed by DREO for use in flight trials. To avoid the long recovery time involved with hard saturation of the analog-to-digital converter in the C/DAQU, a clamping amplifier is required for the last stage in the receive chain of the transceiver. Because no off-the-shelf product was available that would meet the stringent requirements of this application, a clamping amplifier was developed, fabricated, and tested at DREO using in-house laboratory equipment. This technical note outlines the design specifications, the performance issues (dynamic range, third order intermodulation products, and saturation recovery time), and the performance results of the clamping amplifier.

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Missile Approach Warning System
Voltage Feedback Clamping Amplifier
Dynamic Range
Third Order Intermodulation Products
Harmonic Distortion

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